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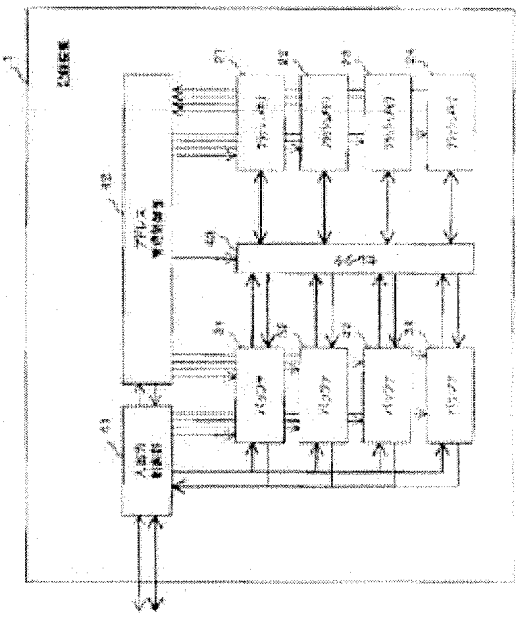
(54) RECORDING DEVICE, RECORDING CONTROL METHOD, AND PROGRAM

(57)Abstract:
PROBLEM TO BE SOLVED: To reduce the frequency of generation of an entrainment saving processing.
SOLUTION: Assuming that the size of all data required for writing from the outside is q, the number of recording media is m, and the size of a block is p, the quotient zm+w+y (z; integer, 0≤z, w; integer, 0≤w<m, y; 0 ≤y<1) is acquired by diving the size of all the data q by the size of the block p. The control is executed so that data in the blocks to the number of zm are written in parallel to the recording media to the number of m, and that thereafter data in the blocks to the number of (q−zm) are written to the recording media to the number of w+1 (where, w in the case of y=0). Resultantly, the frequency of generation of the entrainment saving processing is reduced.



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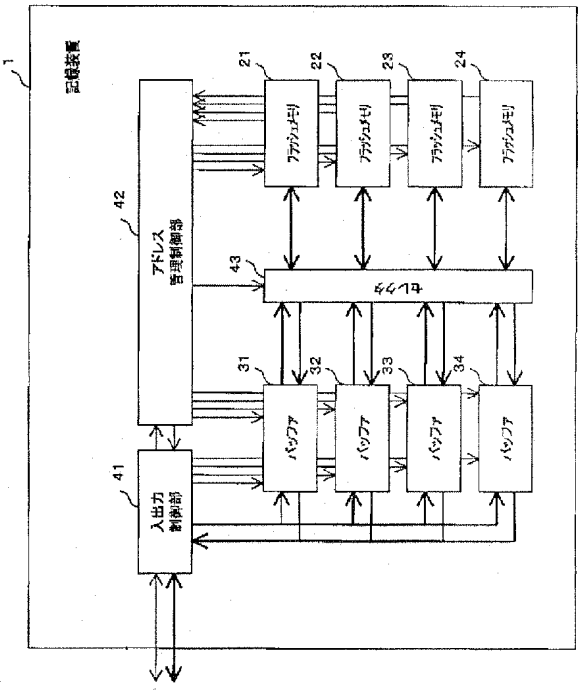
(54)【発明の名称】　記録装置、記録制御方法、及びプログラム

(57)【要約】
【課題】　巻き込み退避処理の発生する頻度を低下させることを目的とする。
【解決手段】　外部から書き込み要求された全データのサイズをｑ、記録媒体の数をｍ、ブロックのサイズをｐとした場合、上記全データのサイズｑを上記ブロックのサイズｐで除してｚｍ＋ｗ＋ｙ（ｚ：０≦ｚの整数，ｗ：０≦ｗ＜ｍの整数，ｙ：０≦ｙ＜１）なる商を得る。そして、ｚｍブロック分のデータをｍ個の記録媒体に対して並列に書き込み、その後、（ｑ－ｚｍ）ブロック分のデータをｗ＋１（但し、ｙ＝０のときはｗ）個の記録媒体に対して書き込むように制御する。このようにすれば、巻き込み退避処理の発生する頻度が低下する。



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【特許請求の範囲】

【請求項１】　消去処理が完了している記録領域に対してデータ書き込みを行い、かつ、複数の記録領域からなる所定のブロック単位で一括してデータ消去を行う複数の記録媒体に対し、外部から書き込み要求されたデータを並列に書き込む記録装置において、

上記外部から書き込み要求された全データのサイズをｑ、上記記録媒体の数をｍ、上記ブロックのサイズをｐとし、上記外部から書き込み要求された全データのサイズｑを上記ブロックのサイズｐで除してｚｍ＋ｗ＋ｙ（ｚ：０≦ｚの整数，ｗ：０≦ｗ＜ｍの整数，ｙ：０≦ｙ＜１）なる商を得たとき、ｚｍブロック分のデータをｍ個の記録媒体に対して並列に書き込み、その後、（ｑ－ｚｍ）ブロック分のデータをｗ＋１（但し、ｙ＝０のときはｗ）個の記録媒体に対して書き込むように制御するアドレス管理制御部を備えたことを特徴とする記録装置。

【請求項２】　上記アドレス管理制御部は、上記（ｑ－ｚｍ）ブロック分のデータをｗ＋１個の記録媒体に対して並列に書き込むように制御する請求項１に記載の記録装置。

【請求項３】　上記アドレス管理制御部は、上記（ｑ－ｚｍ）ブロック分のデータを書き込むに際しては、ｙブロック分のデータを１個の記録媒体に書き込む処理をｗ＋１個の記録媒体に対して並列に実行し、その後、（１－ｙ）ブロック分のデータを１個の記録媒体に書き込む処理をｗ個の記録媒体に対して並列に実行するように制御する請求項１に記載の記録装置。

【請求項４】　上記アドレス管理制御部は、上記（ｑ－ｚｍ）ブロック分のデータをｗ＋１個の記録媒体に割り当てた状態で各記録媒体が持つ順番で書き込むように制御する請求項１に記載の記録装置。

【請求項５】　上記アドレス管理制御部は、書き込み要求先となる記録領域が属するブロック内において、書き換えが必要でないデータが存在する場合は、この書き換えが必要でないデータと当該書き込み要求されたデータとの総和を上記（ｑ－ｚｍ）ブロック分のデータとみなして制御する請求項４に記載の記録装置。

【請求項６】　上記アドレス管理制御部は、書き込み処理が早く終了した記録媒体から順に次のデータを書き込むように制御する請求項１に記載の記録装置。

【請求項７】　上記アドレス管理制御部は、書き込み先でない記録媒体に消去処理の完了していないブロックが存在する場合、該ブロックについての消去処理を当該書き込み処理と並行して行う請求項１に記載の記録装置。

【請求項８】　上記アドレス管理制御部は、外部からアクセス要求される論理アドレスに対応して、

記録媒体を指定するための記録媒体指定情報、データが書き込まれている記録媒体の物理アドレスを示す物理アドレス情報、幾つの記録媒体に対して並列書き込みされたかを示す並列度情報、並列書き込みされていない記録領域の数を示す非並列記録領域数情報、並列書き込みの順番を記録領域単位で表した記録領域列管理情報のうちの少なくとも１つの情報を設定可能な管理テーブルを備えた請求項１に記載の記録装置。

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【請求項９】　消去処理が完了している記録領域に対してデータ書き込みを行い、かつ、複数の記録領域からなる所定のブロック単位で一括してデータ消去を行う複数の記録媒体に対し、外部から書き込み要求されたデータを並列に書き込む記録制御方法において、

上記外部から書き込み要求された全データのサイズをｑ、上記記録媒体の数をｍ、上記ブロックのサイズをｐとし、上記外部から書き込み要求された全データのサイズｑを上記ブロックのサイズｐで除してｚｍ＋ｗ＋ｙ（ｚ：０≦ｚの整数，ｗ：０≦ｗ＜ｍの整数，ｙ：０≦ｙ＜１）なる商を得たとき、ｚｍブロック分のデータをｍ個の記録媒体に対して並列に書き込み、その後、（ｑ－ｚｍ）ブロック分のデータをｗ＋１（但し、ｙ＝０のときはｗ）個の記録媒体に対して書き込むように制御することを特徴とする記録制御方法。

【請求項１０】　消去処理が完了している記録領域に対してデータ書き込みを行い、かつ、複数の記録領域からなる所定のブロック単位で一括してデータ消去を行う複数の記録媒体に対し、外部から書き込み要求されたデータを並列に書き込む記録装置に、

上記外部から書き込み要求された全データのサイズをｑ、上記記録媒体の数をｍ、上記ブロックのサイズをｐとし、上記外部から書き込み要求された全データのサイズｑを上記ブロックのサイズｐで除してｚｍ＋ｗ＋ｙ（ｚ：０≦ｚの整数，ｗ：０≦ｗ＜ｍの整数，ｙ：０≦ｙ＜１）なる商を得たとき、ｚｍブロック分のデータをｍ個の記録媒体に対して並列に書き込み、その後、（ｑ－ｚｍ）ブロック分のデータをｗ＋１（但し、ｙ＝０のときはｗ）個の記録媒体に対して書き込むように制御するアドレス管理制御処理を実行させることを特徴とするプログラム。

【請求項１１】　上記（ｑ－ｚｍ）ブロック分のデータをｗ＋１個の記録媒体に対して並列に書き込むように制御する請求項１０に記載のプログラム。

【請求項１２】　上記（ｑ－ｚｍ）ブロック分のデータを書き込むに際しては、ｙブロック分のデータを１個の記録媒体に書き込む処理をｗ＋１個の記録媒体に対して並列に実行し、その後、（１－ｙ）ブロック分のデータを１個の記録媒体に書き込む処理をｗ個の記録媒体に対して並列に実行するように制御する請求項１０に記載のプログラム。

【請求項１３】　上記（ｑ－ｚｍ）ブロック分のデータをｗ＋１個の記録媒体に割り当てた状態で各記録媒体が持つ順番で書き込むように制御する請求項１０に記載のプログラム。

【請求項１４】　書き込み要求先となる記録領域が属するブロック内において、書き換えが必要でないデータが存在する場合は、この書き換えが必要でないデータと当該書き込み要求されたデータとの総和を上記（ｑ－ｚｍ）ブロック分のデータとみなして制御する請求項１３に記載のプログラム。

【発明の詳細な説明】

【０００１】

【発明の属する利用分野】本発明は、データを記録するための記録装置に関し、特に、フラッシュメモリ等の記録媒体にデータを記録するための記録装置に関する。

【０００２】

【従来の技術】音楽データや映像データを取り扱う携帯機器の記録装置では、①データの書き換えが可能である、②携帯性が高い、③電池等によるバックアップが必要ない等の理由から、フラッシュメモリ等の記録媒体を用いるのが一般的である。

【０００３】しかしながら、現状のフラッシュメモリによると、データ書き込みの際に待ち時間が生じるという問題があった。その理由は、書き込み対象であるデータを記録装置内のバッファへ転送するのに必要な時間よりも、このようにバッファに転送されたデータを当該バッファからフラッシュメモリへ書き込むのに必要な時間の方が大幅に長いためである。

【０００４】そこで、特開２０００－１３２９８２号公報には、複数のフラッシュメモリを備えた記録装置が開示されている。このような記録装置によれば、複数のフラッシュメモリに対して並列にデータ書き込みを行うことができるため、待ち時間が生じるという上記問題は発生しない。

【０００５】

【発明が解決しようとする課題】ところで、一般に、フラッシュメモリへのデータ書き込み単位はセクタと呼ばれ、フラッシュメモリ上のデータ消去（後述する）単位はブロックと呼ばれる。すなわち、図９（ａ）に示すように、フラッシュメモリ内のデータは、３２個のセクタからなるブロックという単位で管理されている（以下、セクタのデータ長は５１２バイト、ブロックのデータ長は１６キロバイトとして説明する）。

【０００６】また、フラッシュメモリには、一方向のデータ書き換えしかできない、すなわち、データの値を１から０へ（或いは０から１へ）書き換えることはできないという特徴がある。従って、データ書き込みを行うには、その書き込み先となる領域内のデータの値を全て１（或いは０）に変換しておく必要がある（以下、この変換処理を「消去処理」という。また、この消去処理が完了している領域を「消去済領域」、完了していない領域を「未消去領域」という）。

【０００７】以上の事情から、図９（ｂ）に示すブロックＡ内のデータ０～１５を書き換える場合は、まず、図９（ｃ）に示すように、書き換える必要のないデータ１６～３１を一旦フラッシュメモリＦ１からバッファＢに読み出す。そして、このようにバッファＢに読み出したデータ１６～３１を、図９（ｄ）に示すように別のフラッシュメモリＦ２の消去済領域Ｅに書き直した後、上記ブロックＡの領域について消去処理を行う。

【０００８】上記一連の処理（すなわち、書き換える必要のないデータ１６～３１が当該書き換え処理に巻き込まれないようにするための処理）は巻き込み退避処理と呼ばれ、フラッシュメモリへの書き込み速度を低下させる大きな要因となっている。なお、図９（ｄ）に示す書き換え後データ０～１５は、外部から当該記録装置に渡されるようになっているが、この点については、ここでは詳しい説明を省略する。

【０００９】ここで、上記したように、特開２０００－１３２９８２号公報に開示される記録装置によれば、複数のフラッシュメモリに対して並列にデータ書き込みを行うことができるため、待ち時間が生じるという上記問題は発生しない。しかしながら、このように複数のフラッシュメモリに対して並列にデータ書き込みを行うと、データ消去の際に巻き込み退避処理の発生する頻度が高くなるという課題があった。

【００１０】すなわち、ある音楽データＭ１をフラッシュメモリに書き込む場合、そのデータサイズが（フラッシュメモリの１ブロックのサイズ）×（フラッシュメモリの個数）の整数倍でないときは、図１０に示すように、フラッシュメモリＦ１～Ｆ４のそれぞれの最終ブロック（後述する）Ｂ１～Ｂ４に空き領域が発生する。その後、当該フラッシュメモリＦ１～Ｆ４に別の音楽データＭ２を書き込む場合、この音楽データＭ２は上記最終ブロックＢ１～Ｂ４の空き領域から書き込まれることになる結果、別個の音楽データＭ１・Ｍ２が同一ブロック内に存在することになる。従って、この状態で音楽データＭ１の全部を消去する必要が生じた場合は、最終ブロックＢ１～Ｂ４に書き込まれた音楽データＭ２を退避させなければならない。

【００１１】なお、上記最終ブロックとは、書き込み対象であるデータが最後に書き込まれることになるブロックをいう。すなわち、図６に示すように、ｍ個のフラッシュメモリに対して並列にデータ書き込みを行うと、一点鎖線より左にハッチングで示すブロックには空き領域が発生しないが、一点鎖線より右にハッチングで示すブロックには空き領域が発生する可能性がある。このように、空き領域が発生する可能性のあるブロックは、書き込み対象であるデータが最後に書き込まれることになるブロックであることから、これらブロックを特に「最終ブロック」と呼ぶことにする。

【００１２】本発明は、上記従来の事情に基づいて提案されたものであって、複数のフラッシュメモリに対して並列にデータ書き込みを行う記録装置において巻き込み

退避処理の発生する頻度を低下させることを目的とする。

【００１３】

【課題を解決するための手段】本発明は、上記目的を達成するために以下の手段を採用している。すなわち、本発明は、図１に示すように、消去処理が完了している記録領域に対してデータ書き込みを行い、かつ、複数の記録領域からなる所定のブロック単位で一括してデータ消去を行う複数の記録媒体２１・２２・２３・２４に対し、外部から書き込み要求されたデータを並列に書き込む記録装置１を前提としている。

【００１４】ここで、上記外部から書き込み要求された全データのサイズをｑ、上記記録媒体の数をｍ、上記ブロックのサイズをｐとした場合、アドレス管理制御部４２は、まず、上記外部から書き込み要求された全データのサイズｑを上記ブロックのサイズｐで除してｚｍ＋ｗ＋ｙ（ｚ：０≦ｚの整数，ｗ：０≦ｗ＜ｍの整数，ｙ：０≦ｙ＜１）なる商を得る。そして、ｚｍブロック分のデータをｍ個の記録媒体に対して並列に書き込み、その後、（ｑ－ｚｍ）ブロック分のデータをｗ＋１（但し、ｙ＝０のときはｗ）個の記録媒体に対して書き込むように制御する。

【００１５】例えば、アドレス管理制御部４２は、図８（ａ）に示すように、上記（ｑ－ｚｍ）ブロック分のデータをｗ＋１個の記録媒体に対して並列に書き込むように制御する。このようにすれば、空き領域の生じるブロックの数は、上記従来技術を適用した場合と比べて少なくなる。これによって、巻き込み退避処理の発生する頻度が低下することになるのはいうまでもない。

【００１６】もちろん、図８（ｂ）に示すように、上記（ｑ－ｚｍ）ブロック分のデータを書き込むに際しては、ｙブロック分のデータを１個の記録媒体に書き込む処理をｗ＋１個の記録媒体に対して並列に実行し、その後、（１－ｙ）ブロック分のデータを１個の記録媒体に書き込む処理をｗ個の記録媒体に対して並列に実行するように制御するようにしてもよい。このようにすれば、空き領域の生じるブロックは多くても１個となるため、巻き込み退避処理の発生する頻度はさらに低下する。

【００１７】あるいは、図８（ｃ）に示すように、上記（ｑ－ｚｍ）ブロック分のデータをｗ＋１個の記録媒体に割り当てた状態で各記録媒体が持つ順番で書き込むように制御するようにしてもよい。この制御方法は、書き込み要求先となる記録領域が属するブロック内に「書き換えが必要でないデータ」が存在する場合、特に有効である。すなわち、このような場合、アドレス管理制御部４２は、上記書き換えが必要でないデータと当該書き込み要求されたデータとの総和を上記（ｑ－ｚｍ）ブロック分のデータとみなして制御するようになっている。

【００１８】

【発明の実施の形態】図１は、本発明を適用した記録装置のブロック図であり、以下その構成を説明する。なお、以下の説明では、セクタのデータ長は５１２バイト、ブロックのデータ長は１６キロバイトであることを前提にする。

【００１９】まず、入出力制御部４１は、データの書き込み・読み出し・消去等の処理要求を外部から受けると、当該処理の開始命令をアドレス管理制御部４２に出すとともに、以下のデータ入出力制御を行う。

【００２０】すなわち、データの書き込み要求を受けた入出力制御部４１は、外部から入力されたデータを複数のバッファ３１・３２・３３・３４に５１２バイト単位で順次書き込む。一方、データの読み出しの要求を受けた入出力制御部４１は、複数のバッファ３１・３２・３３・３４から５１２バイト単位で順次データを読み出して外部に出力する。

【００２１】また、アドレス管理制御部４２は、上記入出力制御部４１からの処理開始命令に応じ、複数のフラッシュメモリ２１・２２・２３・２４と複数のバッファ３１・３２・３３・３４との間でのデータ転送の制御と、複数のフラッシュメモリ２１・２２・２３・２４に対するデータ消去の制御と、複数のフラッシュメモリ２１・２２・２３・２４に書き込まれているデータの管理とを行う（詳細は後述する）。

【００２２】更に、セレクタ４３は、上記アドレス管理制御部４２からの接続切り替え信号に応じ、複数のフラッシュメモリ２１・２２・２３・２４と複数のバッファ３１・３２・３３・３４との間のデータバスの接続を切り替える。

【００２３】ここで、上記アドレス管理制御部４２が行うデータ書き込み制御方法は、以下の２パターンに大別される。すなわち、一つは、未だデータの書き込まれていない論理アドレス領域に対してデータ書き込み要求を受けた場合の制御方法（以下「第１のデータ書き込み制御方法」という）であり、もう一つは、既にデータの書き込まれている論理アドレス領域に対してデータ書き込み要求を受けた場合の制御方法（以下「第２のデータ書き込み制御方法」という）である。

【００２４】以下、これらデータ書き込み制御方法を詳細に説明する。

〔第１のデータ書き込み制御方法〕まず、データの書き込まれていない論理アドレス領域に対してデータ書き込み要求を受けた場合、上記従来と同様、４個のフラッシュメモリ２１・２２・２３・２４に対して並列にデータ書き込みを行っていく。ただし、本発明では、当該書き込み対象であるデータのサイズによって、図２（ａ）～（ｃ）に示すように、フラッシュメモリ２１・２２・２３・２４それぞれの最終ブロックへの書き込み制御方法が異なる。

【００２５】例えば、書き込み対象であるデータのサイズが６４キロバイトである場合は、このデータを４個の

フラッシュメモリ２１・２２・２３・２４へ並列に書き込んでも、その最終ブロックＢ２１・Ｂ２２・Ｂ２３・Ｂ２４のいずれにも空き領域は生じない。これは、上記６４キロバイトのデータが４ブロックに相当し、最終ブロックＢ２１・Ｂ２２・Ｂ２３・Ｂ２４の総和と一致するからである。

【００２６】従って、この場合のアドレス管理制御部４２は、図２（ａ）に示すように、４個の最終ブロックＢ２１・Ｂ２２・Ｂ２３・Ｂ２４に対してデータ０～１２７を並列に書き込むように制御する（以下、この書き込み形態を「４ブロック書き込み」という）。

【００２７】また、書き込み対象であるデータのサイズが３２キロバイトである場合は、このデータを４個のフラッシュメモリ２１・２２・２３・２４へ並列に書き込むと、その最終ブロックＢ２１・Ｂ２２・Ｂ２３・Ｂ２４それぞれに１／２ブロックの空き領域が発生する。これは、上記３２キロバイトのデータが２ブロックに相当し、最終ブロックＢ２１・Ｂ２２・Ｂ２３・Ｂ２４の総和の１／２倍に一致するからである。

【００２８】従って、この場合のアドレス管理制御部４２は、図２（ｂ）に示すように、２個の最終ブロックＢ２１・Ｂ２２に対してのみデータ０～６３を並列に書き込むように制御する。すなわち、空き領域が生じることを防止する関係上、最終ブロックＢ２１・Ｂ２２・Ｂ２３・Ｂ２４への書き込みについては並列度を４から２に制限するようになっている（以下、この書き込み形態を「２ブロック書き込み」という）。

【００２９】ここで、書き込み対象であるデータのサイズが２４キロバイトである場合は、上記３２キロバイトの場合のように並列度を制限しても、最終ブロックに空き領域が生じることを防止できない。これは、上記２４キロバイトのデータが１．５ブロックに相当し、ブロックの整数倍に一致しないからである。

【００３０】従って、この場合のアドレス管理制御部４２は、図２（ｃ）に示すように、空き領域の生じる最終ブロックが１個だけになるように、また、可能な限り並列書き込みとなるようにデータ０～４７を制御する。

【００３１】すなわち、１ブロック分のデータ０～３１を２個の最終ブロックＢ２１・Ｂ２２に対して並列に書き込んだ後、残り０．５ブロック分の端数データ３２～４７を１個の最終ブロックＢ２１に対して単一に書き込むようになっている（以下、この書き込み形態を「１．５ブロック書き込み」という）。なお、「単一に書き込む」とは、並列書き込みを並列度１で行うことをいう。

【００３２】以上のように、アドレス管理制御部４２は、書き込み対象であるデータのサイズに応じた制御方法を判別するようになっており、以下、その判別手法について説明する。

【００３３】まず、書き込み要求された全データのサイズをｑ、フラッシュメモリの数をｍ、ブロックのサイズをｐとした場合、この全データのサイズｑを上記ブロックのサイズｐで除して、ｚｍ＋ｗ＋ｙ（ｚ：０≦ｚの整数，ｗ：０≦ｗ＜ｍの整数，ｙ：０≦ｙ＜１）なる商を得る。

【００３４】ここで、上記ｚｍは、並列度がｍのブロック数を意味し、上記ｗ＋ｙは、並列度がｍに至らないブロック数を意味する。すなわち、図６を用いて説明すると、一点鎖線より左にハッチングで示すブロックの数が上記ｚｍに相当し、一点鎖線より右にハッチングで示すブロックの数が上記ｗ＋ｙに相当する（なお、ｗはブロックＢ１ に対応し、ｙはブロックＢ２ に対応する）。

【００３５】従って、アドレス管理制御部４２は、ｚｍブロック分のデータをｍ個のフラッシュメモリに対して並列に書き込み、その後、ｑ－ｚｍブロック分のデータをｗ＋１（但し、ｙ＝０のときはｗ）個のフラッシュメモリに対して書き込むように制御する。ただし、この（ｑ－ｚｍ）ブロック分のデータを書き込むに際しては、ｙブロック分のデータを１個のフラッシュメモリに書き込む処理をｗ＋１個のフラッシュメモリに対して並列に実行し、その後、（１－ｙ）ブロック分のデータを１個のフラッシュメモリに書き込む処理をｗ個のフラッシュメモリに対して並列に実行するようになっている。

【００３６】以下、上記判別手法の具体例として、１ブロックが１６キロバイトである状況下、４個のフラッシュメモリに対して１５２キロバイトのデータを書き込む場合（ｐ＝１６、ｍ＝４、ｑ＝１５２の場合）の制御手順について説明する。

【００３７】まず、ｑ÷ｐ＝ｚｍ＋ｗ＋ｙは１５２÷１６＝２×４＋１＋０．５であることから、ｚは２、ｗは１、ｙは０．５であることが判る。

【００３８】従って、２ブロック分のデータを４個のフラッシュメモリに対して並列に書き込み、その後、１．５ブロック分のデータを２個のフラッシュメモリに対して書き込む。ただし、この１．５ブロック分のデータを書き込むに際しては、０．５ブロック分のデータを１個のフラッシュメモリに書き込む処理を２個のフラッシュメモリに対して並列に実行し、その後、（１－０．５）ブロック分のデータを１個のフラッシュメモリに書き込む処理を１個のフラッシュメモリに対して並列に実行する。すなわち、図６でいうと、ブロックＢ１ とＢ２ それぞれに対して０．５ブロック分のデータを並列に書き込み、その後、ブロックＢ１ に対してのみ０．５ブロック分のデータを単一に書き込むことになる。

【００３９】なお、ここでは、書き込み要求された全データのサイズｐを１５２キロバイト、また、ブロックのサイズｑを１６キロバイトとして説明したが、このサイズｐ及びｑの単位はバイトに限定されるものではない。例えば、書き込み要求された全データのサイズｐを３０４セクタ、また、ブロックのサイズｑを３２セクタとしても上記と同様の効果が得られる。

【００４０】以上説明したように、本発明によれば、空き領域の生じるブロックは多くても１個となる。これによって、巻き込み退避処理の発生する頻度が低下する結果、トータルでみると、フラッシュメモリへの書き込みパフォーマンスを向上させることが可能である。

【００４１】もっとも、本発明によると並列度が制限される場合もあり、この点では書き込み速度の低下を招く。しかしながら、並列度が制限されるのは最終ブロックについてのみであり、また、この最終ブロックについても可能な限り並列書き込みを行うようにしているので、上記のように並列度が制限されたとしても、その書き込み速度への影響は極めて小さい。

【００４２】なお、上記の説明では、フラッシュメモリ２１→２２→２３→２４→２１→・・・の順に並列書き込みを行う動作について説明したが、本発明はこれに限定されるものではない。すなわち、個々のフラッシュメモリのハードウェア性能にはバラツキがあるため、それぞれの書き込み処理に要する時間にもバラツキがある。従って、上記のように並列書き込みを行うのではなく、書き込み処理が早く終了したフラッシュメモリから順に、次のデータを書き込むように制御するのが好ましい。

【００４３】また、図２（ｂ）（ｃ）に示したように、書き込み対象であるデータのサイズが３２キロバイトや２４キロバイトである場合は、並列度が２に制限されている期間、すなわち、２個のフラッシュメモリ２１・２２に対してのみ並列書き込み処理が行われている期間が存在する。従って、残り２個のフラッシュメモリ２３・２４内に未消去領域が存在する場合は、この領域の消去処理を、上記フラッシュメモリ２１・２２に対する書き込み処理と並行して行うのが好ましい。

【００４４】更に、上記の説明では、（ｑ－ｚｍ）ブロック分のデータを書き込むに際しては、ｙブロック分のデータを１個のフラッシュメモリに書き込む処理をｗ＋１個のフラッシュメモリに対して並列に実行し、その後、（１－ｙ）ブロック分のデータを１個のフラッシュメモリに書き込む処理をｗ個のフラッシュメモリに対して並列に実行することとしているが、本発明はこれに限定されるものではない。すなわち、図８（ａ）に示すように、上記（ｑ－ｚｍ）ブロック分のデータをｗ＋１個のフラッシュメモリに対して並列に書き込むようにしてもよい。

【００４５】もっとも、このようにすると、空き領域の生じるブロックの数は２個以上になる場合がある。しかしながら、その数は、上記従来技術を適用した場合と比べると少なくなるのはいうまでもない。

【００４６】ところで、上記のように並列に書き込んだデータを読み出したり書き換えたりするためには、当該フラッシュメモリ２１・２２・２３・２４におけるデータ書き込み状態をアドレス管理制御部４２が統括して管理しておかなければならない。すなわち、アドレス管理制御部４２は、外部からアクセス要求される論理アドレスブロック毎に、以下のフィールドを備えたブロック管理テーブル（図３参照）を生成するようになっている。

【００４７】まず、並列度フィールドとは、幾つのフラッシュメモリに対して並列にデータが書き込まれたかを示すフィールドをいう。すなわち、上記のように４ブロック書き込みされた論理アドレスブロックの並列度フィールドには、図３（ａ）に示すように「４」を設定する。一方、上記のように２ブロック書き込み及び１．５ブロック書き込みされた論理アドレスブロックの並列度フィールドには、図３（ｂ）（ｃ）に示すように「２」を設定する。なお、未書き込み領域である論理アドレスブロックの並列度フィールドには「０」を設定しておく。

【００４８】次に、非並列セクタ数フィールドとは、当該論理アドレスブロックに含まれる３２個のセクタのうち、並列書き込みが行われていないセクタの数を示すフィールドをいう。すなわち、上記のように４ブロック書き込み及び２ブロック書き込みされた論理アドレスブロックの非並列セクタ数フィールドには、図３（ａ）（ｂ）に示すように「０」を設定する。一方、上記のように１．５ブロック書き込みされた論理アドレスブロックの非並列セクタ数フィールドには、図３（ｃ）に示すように「１６」を設定する。

【００４９】次に、フラッシュメモリ指定フィールドとは、当該論理アドレスブロックが存在するフラッシュメモリを示すフィールドをいう。例えば、上記フラッシュメモリ２１内に存在する論理アドレスブロックのフラッシュメモリ指定フィールドには「０」を設定し、上記フラッシュメモリ２２内に存在する論理アドレスブロックのフラッシュメモリ指定フィールドには「１」を設定する。また、上記フラッシュメモリ２３内に存在する論理アドレスブロックのフラッシュメモリ指定フィールドには「２」を設定し、上記フラッシュメモリ２４内に存在する論理アドレスブロックのフラッシュメモリ指定フィールドには「３」を設定する。

【００５０】次に、物理アドレスフィールドとは、当該論理アドレスブロックに対応する物理アドレスを示すフィールドをいう。もちろん、このフィールドに設定する物理アドレスは、上記フラッシュメモリ指定フィールドに示されるフラッシュメモリ内の物理アドレスである。

【００５１】次に、セクタ列管理情報フィールドとは、並列書き込みの順番をセクタ単位で表したフィールドをいう。例えば、フラッシュメモリ２１→２２→２３→２４→２１→・・・の順に並列書き込みを行った場合は、図３（ａ）に示すように、論理アドレスａに対応するセクタ列管理情報として「０」が、論理アドレスａ＋１に対応するセクタ列管理情報として「１」が、論理アドレスａ＋２に対応するセクタ列管理情報として「２」が、

論理アドレスａ＋３に対応するセクタ列管理情報として「３」が、それぞれ並ぶことになる。

〔第２のデータ書き込み制御方法〕ところで、フラッシュメモリに書き込むデータは、一連の画像データや音楽データ（１画像ファイルや１音楽ファイル）であるのが通常である。従って、フラッシュメモリに書き込まれたデータを消去する場合も、一連の画像データや音楽データ（すなわち、連続して書き込まれたデータ）を一括して消去する可能性が高い。そこで、上記第１のデータ書き込み制御では、書き込み速度を低下させない観点から、可能な限り並列書き込みを行うこととしている。

【００５２】しかしながら、上記第１のデータ書き込み制御方法のように可能な限り並列書き込みを行うよりも、単一に書き込んだ方が、トータルでみるとフラッシュメモリへの書き込みパフォーマンスが向上する場面もある。

【００５３】例えば、フラッシュメモリに書き込んだ音楽データの編集作業においては、連続して書き込まれたデータの一部を書き換えたい場合がある。この場合、書き換え対象であるデータは、図７（ａ）にハッチング領域として示すように複数のブロックにわたって書き込まれているよりも、図７（ｂ）にハッチング領域として示すように１個のブロックに書き込まれている方がよい。なぜなら、図７（ａ）に示す場面では、４個のブロックについて巻き込み退避処理をする必要があるのに対し、図７（ｂ）に示す場面では、１個のブロックについて巻き込み退避処理をすればよいためである。

【００５４】このようなことから、上記第１のデータ書き込み制御方法によって複数のフラッシュメモリへ連続データを並列に書き込んだ後、万一、この連続データの一部を書き換える必要が生じた場合は、以下の制御方法を採用するのが好ましい。

【００５５】まず、データ書き込み要求を受けたアドレス管理制御部４２は、上記ブロック管理テーブルの内容を参照することによって、このデータ書き込み要求が、連続データの一部を書き換えるための要求（以下「データ書き換え要求」という場合がある）、あるいは、新規に連続データを書き込むための要求（以下「新規データ書き込み要求」という場合がある）のいずれであるかを判断する。すなわち、既にデータの書き込まれている論理アドレス領域に対するデータ書き込み要求であれば、当該データ書き込み要求はデータ書き換え要求であると判断し、一方、未だデータの書き込まれていない論理アドレス領域に対するデータ書き込み要求であれば、当該データ書き込み要求は新規データ書き込み要求であると判断するようになっている。

【００５６】そして、当該データ書き込み要求は新規データ書き込み要求であると判断したアドレス管理制御部４２は、上記第１のデータ書き込み制御方法を採用するようになっている。一方、当該データ書き込み要求はデータ書き換え要求であると判断したアドレス管理制御部４２は、更に、書き換え対象であるデータが属するブロック内において、書き換えが必要でないデータが存在するか否かを判断する。

【００５７】例えば、図４に示すように、データ０～４７がフラッシュメモリ２１・２２に１．５ブロック書き込みされている状況下、データ３２～４７を書き換えるための要求があった場合は、データ３２～４７が属するブロック内において、書き換えが必要でないデータ０～３１（但し、奇数を除く）が存在する。従って、この場合のアドレス管理制御部４２は「書き換えが必要でないデータが存在する」と判断することになり、以下の制御を行う。

【００５８】まず、アドレス管理制御部４２は、書き換えが必要でないデータ０～３１（３２個のセクタデータ）と、当該書き込み要求されたデータ３２～４７（１６個のセクタデータ）との総和である１．５ブロック分のデータを上記（ｑ－ｚｍ）ブロック分のデータとみなす。このとき、ｗは１であり、またｙは０．５であることはいうまでもない。

【００５９】そして、アドレス管理制御部４２は、この（ｑ－ｚｍ）ブロック分のデータをｗ＋１個のフラッシュメモリ２３・２４に割り当てた状態で、各フラッシュメモリ２３・２４が持つ順番（ここでは２３→２４の順番）で書き込むように制御する。すなわち、２個のブロックに対して並列に書き込まれているデータ０～３１を一旦バッファ３３に読み出した後、フラッシュメモリ２３の消去済領域へ単一に書き直し、次いでデータ３２～４７をフラッシュメモリ２４の消去済領域へ単一に書き込むように制御するようになっている。なお、このデータ３２～４７は、外部から入出力制御部４１・バッファ３４を介してアドレス管理制御部４２に渡されるようになっている。

【００６０】以上のように、第２のデータ書き込み制御によれば、フラッシュメモリ２３・２４上のブロックには可能な限り連続データが並ぶことになる。このようにしておけば、データ０～３１或いはデータ３２～４７を再度書き換える必要が生じた場合、巻き込み退避処理は発生しない。

【００６１】なお、上記では、「書き換えが必要でないデータが存在する」とアドレス管理制御部４２が判断した場合の動作についてのみ説明した。すなわち、「書き換えが必要でないデータが存在しない」とアドレス管理制御部４２が判断した場合の動作については言及していないが、このように判断した場合のアドレス管理制御部４２は、上記第１のデータ書き込み制御方法を採用するようになっている。

【００６２】その理由は、「書き換えが必要でないデータが存在しない」とは、データの全部を書き換えることを意味するからである。例えば、１．５ブロックの領域

に対して２ブロック分のデータ書き込み要求があるということは、以前の１．５ブロック分のデータが不用であることを意味する。従って、このようなデータ書き込み要求は、新規に連続データを書き込むための要求であると考えるのが妥当である。

【００６３】最後に、上記した第２のデータ書き込み制御例によってブロック管理テーブルの内容がどのように遷移するかを図５に示す。なお、フィールド構成や設定情報については、上記第１のデータ書き込み制御と同じであるため、ここでは説明を省略する。

【図面の簡単な説明】

【図１】本発明を適用した記録装置のブロック図

【図２】第１のデータ書き込み制御方法の説明図

【図３】第１のデータ書き込み制御時におけるブロック管理テーブルの状態図

【図４】第２のデータ書き込み制御方法の説明図

【図５】第２のデータ書き込み制御時におけるブロック管理テーブルの状態図

【図６】データ書き込み制御方法の判別手法の説明図　＊

＊【図７】データ書き換えの説明図

【図８】（ｑ－ｚｍ）ブロック分のデータの書き込み態様を示す図

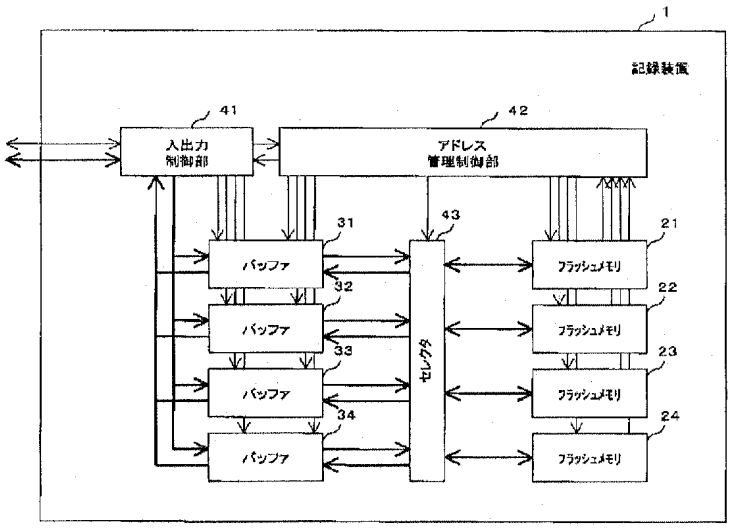
【図９】ブロック・セクタ・巻き込み退避処理の説明図

【図１０】別個のデータが存在するブロックの説明図

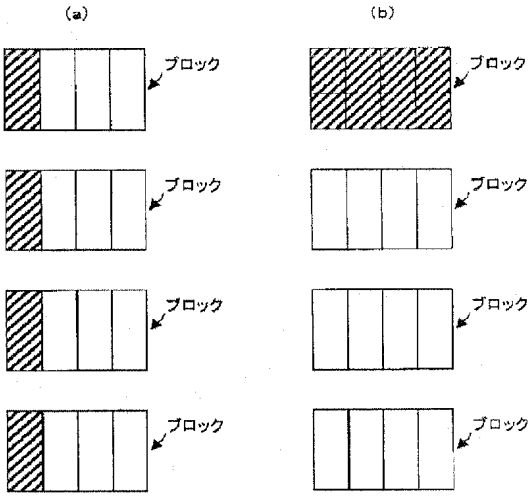
【符号の説明】

１　記録装置
２１　フラッシュメモリ
２２　フラッシュメモリ
２３　フラッシュメモリ
２４　フラッシュメモリ
３１　バッファ
３２　バッファ
３３　バッファ
３４　バッファ
４１　入出力制御部
４２　アドレス管理制御部
４３　セレクタ

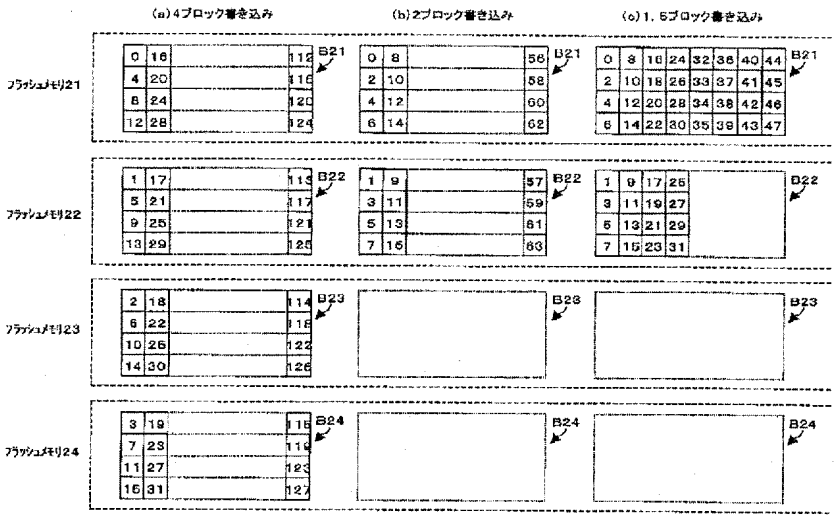
【図１】



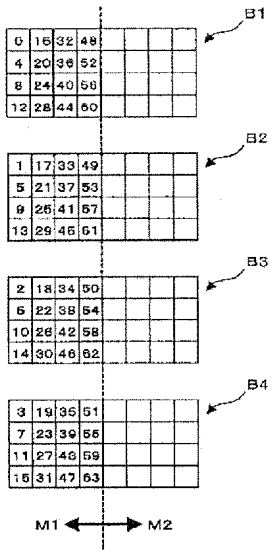
【図７】



【図２】



【図１０】



【図３】

(a)4ブロック書き込み

論理アドレス	並列度	非並列セクタ数	フラッシュメモリ指定	物理アドレス	セクタ列管理情報
a	4	0	0	A	0,0,0,.....,0
a+1	4	0	1	B	1,1,1,.....,1
a+2	4	0	2	C	2,2,2,.....,2
a+3	4	0	3	D	3,3,3,.....,3

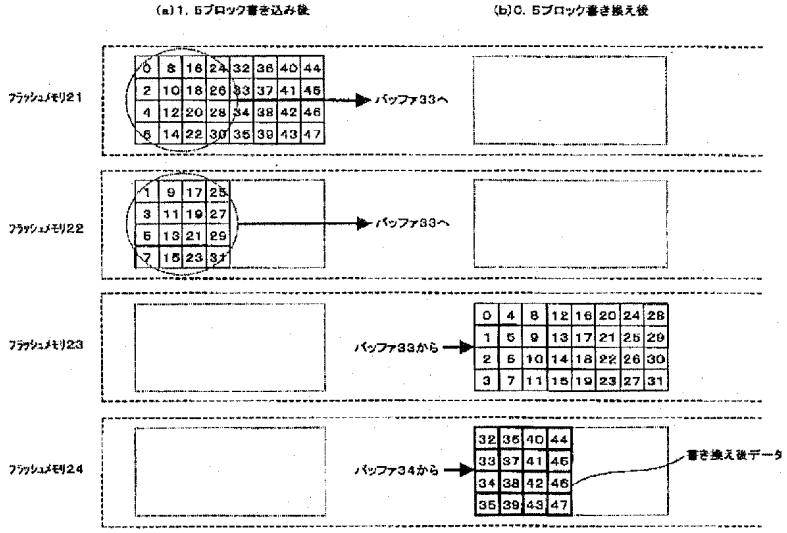
(b)2ブロック書き込み

論理アドレス	並列度	非並列セクタ数	フラッシュメモリ指定	物理アドレス	セクタ列管理情報
b	2	0	0	E	0,0,0,.....,0
b+1	2	0	1	F	1,1,1,.....,1

(c)1.5ブロック書き込み

論理アドレス	並列度	非並列セクタ数	フラッシュメモリ指定	物理アドレス	セクタ列管理情報
c	2	16	0	G	0,0,0,.....,0
c+1	2	16	1	H	1,1,1,.....,1

【図４】



【図５】

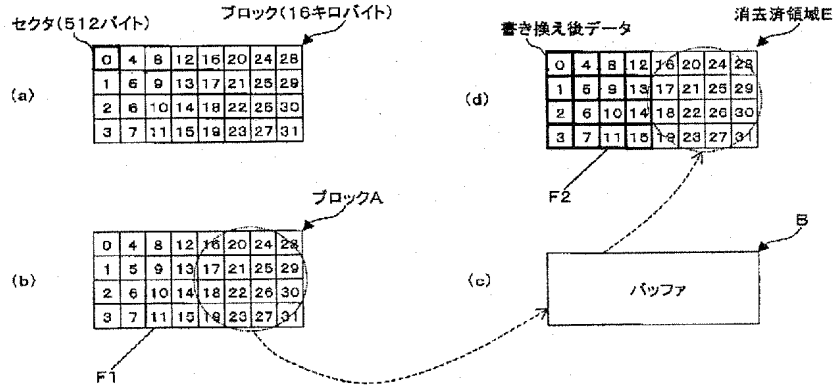
(a)1.5ブロック書き込み後

論理アドレス	並列度	非並列セクタ数	フラッシュメモリ指定	物理アドレス	セクタ列管理情報
c	2	16	0	G	0,0,0,.....,0
c+1	2	16	1	H	1,1,1,.....,1

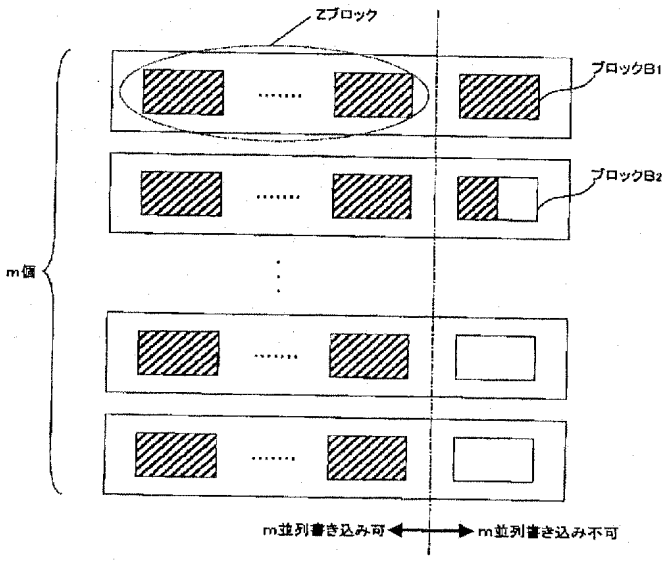
(b)0.5ブロック書き換え後

論理アドレス	並列度	非並列セクタ数	フラッシュメモリ指定	物理アドレス	セクタ列管理情報
c	1	0	2	I	0,0,0,.....,0
c+1	1	0	3	J	0,0,0,.....,0

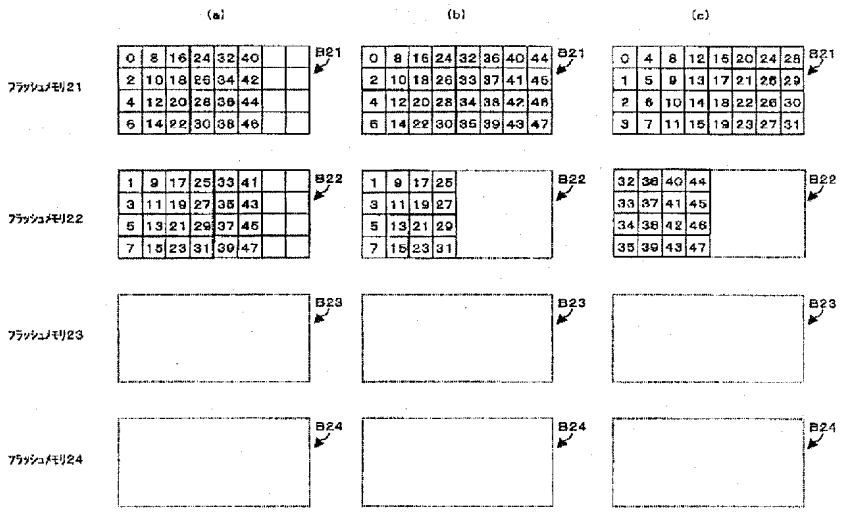
【図９】



【図６】


Zブロック
ブロックB1
ブロックB2
m個
m並列書き込み可
m並列書き込み不可

【図８】


(a)
(b)
(c)
フラッシュメモリ21
フラッシュメモリ22
フラッシュメモリ23
フラッシュメモリ24
B21
B22
B23
B24

* NOTICES *

CLAIMS

[Claim(s)]
[Claim 1]data writing to a record section which erasing processing has completed, [perform and] In recording equipment which writes in in parallel data by which the write request was carried out from the outside to two or more recording media which bundle up by a predetermined block unit which consists of two or more record sections, and perform data erasure, The number of q and the above-mentioned recording media for size of all the data by which the write request was carried out from the above-mentioned outside m, **(ing) size q of all the data by which set size of the above-mentioned block to p, and the write request was carried out from the above-mentioned outside in the size p of the above-mentioned block -- zm+w+y (an integer of z:0 <=z, an integer of w:0 <=w<m, y:0<=y<1), when a quotient is obtained, Recording equipment provided with an address administration control section controlled to write in data for zm block in parallel to m recording media, and to write in data blocked (q-zm) after that to a recording medium of w+1 (at however, the time of y= 0 w) individual.
[Claim 2]The recording equipment according to claim 1 controlled so that the above-mentioned address administration control section writes in data for the above-mentioned (q-zm) block in parallel to w+1 recording medium.
[Claim 3]The above-mentioned address administration control section is faced writing in data for the above-mentioned (q-zm) block, and performs in parallel processing which writes data for y blocks in one recording medium to w+1 recording medium.
Then, the recording equipment according to claim 1 controlled to perform in parallel processing which writes data blocked (1-y) in one recording medium to w recording media.

[Claim 4]The recording equipment according to claim 1 controlled to write in the above-mentioned address administration control section in turn which each recording medium has where data for the above-mentioned (q-zm) block is assigned to w+1 recording medium.
[Claim 5]When data for which rewriting is not required in a block with which a record section used as the write request point belongs exists, the above-mentioned address administration control section, The recording equipment according to claim 4 which considers that total with data for which this rewriting is not required, and the data concerned by which the write request was carried out is data for the above-mentioned (q-zm) block, and controls it.
[Claim 6]The recording equipment according to claim 1 controlled so that the above-mentioned address administration control section writes in the following data sequentially from a recording medium which writing processing ended early.
[Claim 7]The recording equipment according to claim 1 with which the above-mentioned

address administration control section performs erasing processing about this block in parallel to the writing processing concerned when a block which has not completed erasing processing exists in a recording medium which is not a writing destination.
[Claim 8]The above-mentioned address administration control section corresponds to a logical address by which an access request is carried out from the outside, Recording-medium specification information for specifying a recording medium, physical address information which shows a physical address of a recording medium with which data is written in, The degree information of parallel which shows to how many recording media parallel writing was carried out, un-parallel record section number information which shows the number of record sections by which parallel writing is not carried out, The recording equipment according to claim 1 provided with a management table which can set up at least one information in record section sequence management information which expressed turn of parallel writing per record section.
[Claim 9]data writing to a record section which erasing processing has completed, [perform and] In a record control method which writes in in parallel data by which the write request was carried out from the outside to two or more recording media which bundle up by a predetermined block unit which consists of two or more record sections, and perform data erasure, The number of q and the above-mentioned recording media for size of all the data by which the write request was carried out from the above-mentioned outside m, **(ing) size q of all the data by which set size of the above-mentioned block to p, and the write request was carried out from the above-mentioned outside in the size p of the above-mentioned block -- zm+w+y (an integer of z:0 <=z, an integer of w:0 <=w<m, y:0<=y<1), when a quotient is obtained, A record control method controlling to write in data for zm block in parallel to m recording media, and to write in data blocked (q-zm) after that to a recording medium of w+1 (at however, the time of y= 0 w) individual.
[Claim 10]data writing to a record section which erasing processing has completed, [perform and] As opposed to two or more recording media which bundle up by a predetermined block unit which consists of two or more record sections, and perform data erasure, To recording equipment which writes in in parallel data by which the write request was carried out from the outside, size of all the data by which the write request was carried out from the above-mentioned outside q, **(ing) size q of all the data by which set size of m and the above-mentioned block to p, and the write request was carried out from the above-mentioned outside in the number of the above-mentioned recording media in the size p of the above-mentioned block -- zm+w+y (an integer of z:0 <=z, an integer of w:0 <=w<m, y:0<=y<1), when a quotient is obtained, A program performing address administration control management controlled to write in data for zm block in parallel to m recording media, and to write in data blocked (q-zm) after that to a recording medium of w+1 (at however, the time of y= 0 w) individual.
[Claim 11]The program according to claim 10 controlled to write in data for the above-mentioned (q-zm) block in parallel to w+1 recording medium.
[Claim 12]It faces writing in data for the above-mentioned (q-zm) block, The program according to claim 10 controlled to perform in parallel processing which writes data for y blocks in one recording medium to w+1 recording medium, and to perform after that processing which writes data blocked (1-y) in one recording medium in parallel to w recording media.
[Claim 13]The program according to claim 10 controlled to write in in turn which each recording medium has where data for the above-mentioned (q-zm) block is assigned to w+1 recording medium.
[Claim 14]When data for which rewriting is not required in a block with which a record section

used as the write request point belongs exists, The program according to claim 13 which considers that total with data for which this rewriting is not required, and the data concerned by which the write request was carried out is data for the above-mentioned (q-zm) block, and controls it.

[Translation done.] * NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[The field of the invention to which invention belongs] This invention relates to the recording equipment for recording data on recording media, such as a flash memory, especially about the recording equipment for recording data.
[0002]
[Description of the Prior Art]It is common that backup by ** cell with high ** portability which can rewrite ** data, etc. uses recording media, such as a flash memory, from unnecessary Reasons in the recording equipment of the portable device which deals with music data and picture image data.
[0003]However, according to the present flash memory, there was a problem that waiting time arose, on the occasion of data writing. The direction of time required for the Reason to write the data transmitted to the buffer in this way than time required to transmit the data which is a write-in object to the buffer in recording equipment in a flash memory from the buffer concerned is because it is substantially long.
[0004]Then, JP,2000-132982,A has disclosed recording equipment provided with two or more flash memories. According to such recording equipment, since data writing can be performed in parallel to two or more flash memories, the above-mentioned problem that waiting time arises is not generated.
[0005]
[Problem to be solved by the invention]By the way, generally, the data writing unit to a flash memory is called a sector, and the data erasure (it mentions later) unit on a flash memory is called a block. That is, as shown in drawing 9 (a), the data in a flash memory is managed in the unit of the block which consists of 32 sectors (the data length of a sector explains the data length of 512 bytes and a block as 16 K bytes hereafter).
[0006]Only the data rewrite of one way can be performed, i.e., there is the feature that the value of data cannot be rewritten from 1 to 0 (or 0-1) in a flash memory. Therefore, in order to perform data writing, it is necessary to change all the values of the data in the field used as that writing

destination into 1 (or 0) (this conversion process is hereafter called "erasing processing".). The field which this erasing processing has completed is called "eliminated field", and the field which has not been completed is called "uneliminated field."
[0007]When rewriting the data 0-15 within the block A shown in drawing 9 (b) from the above situation, as shown in drawing 9 (c), the data 16-31 which does not need to be rewritten is once first read from flash memory F1 to the buffer B. And as shown the data 16-31 read to the buffer B in this way in drawing 9 (d), after rewriting to the eliminated field E of another flash memory F2, erasing processing is performed about the field of the above-mentioned block A.
[0008]A series of above-mentioned processings (namely, processing for the data 16-31 which does not need to be rewritten not to be involved in the rewriting processing concerned) are called a contamination saving process, and have become a major factor which reduces the drawing speed to a flash memory. Although the after-rewriting data 0-15 shown in drawing 9 (d) is passed to the recording equipment concerned from the exterior, it omits detailed explanation about this point here.
[0009]Here, since data writing can be performed in parallel to two or more flash memories according to the recording equipment indicated by JP,2000-132982,A as described above, the above-mentioned problem that waiting time arises is not generated. However, when data writing was performed in parallel to two or more flash memories in this way, SUBJECT that the frequency which is involved in in the case of data erasure and a saving process generates became high occurred.
[0010]Namely, when writing a certain music data M1 in a flash memory and the data size is not an integral multiple of x (size which is 1 block of a flash memory) (number of a flash memory), as shown in drawing 10, Free space occurs in each final block (it mentions later) B1 - B4 of flash memory F1 - F4. Then, when writing another music data M2 in the flash memory F1 concerned - F4, as a result of writing in this music data M2 from the free space of the above-mentioned final block B1 - B4, the separate music data M1 and M2 will exist in the same block. Therefore, when all of the music data M1 need to be eliminated in this state, the music data M2 written in the final block B1 - B4 must be evacuated.
[0011]The above-mentioned final block means a block with which data which is a write-in object will be written in at the end. That is, as shown in drawing 6, if data writing is performed in parallel to m flash memories, free space will not occur in a block shown by hatching on the left of an alternate long and short dash line, but free space may occur in a block shown by hatching on the right of an alternate long and short dash line. Thus, since data which is a write-in object is the block which will be written in at the end, a block which free space may generate is carried out to calling especially these blocks a "final block."
[0012]This invention was proposed based on the above-mentioned conventional situation, and is ****. The purpose is to reduce frequency which is involved in in recording equipment which performs data writing in parallel to a flash memory, and a saving process generates.

[0013]
[Means for solving problem]The following means are used for this invention to achieve the above objects. Namely, as this invention is shown in drawing 1, data writing is performed to a record section which erasing processing has completed, And it is premised on the recording equipment 1 which writes in in parallel data by which the write request was carried out from the outside to two or more recording media 21, 22, 23, and 24 which bundle up by a predetermined block unit which consists of two or more record sections, and perform data erasure.

[0014]When size of m and the above-mentioned block is set to p for the number of q and the above-mentioned recording media, here the size of all the data by which the write request was carried out from the above-mentioned outside the address administration control section 42, first -- **(ing) size q of all the data by which the write request was carried out from the above-mentioned outside in the size p of the above-mentioned block -- zm+w+y (the integer of z:0 <=z, the integer of w:0 <=w<m, y:0<=y<1) -- a quotient is obtained. And it controls to write in the data for zm block in parallel to m recording media, and to write in data blocked (q-zm) after that to the recording medium of w+1 (at however, the time of y= 0 w) individual.
[0015]For example, the address administration control section 42 is controlled to write in the data for the above-mentioned (q-zm) block in parallel to w+1 recording medium to be shown in drawing 8 (a). If it does in this way, the number of the blocks which free space produces will decrease compared with the case where the above-mentioned conventional technology is applied. It cannot be overemphasized that the frequency which a contamination saving process generates will fall by this.
[0016]Of course, as shown in drawing 8 (b), it faces writing in the data for the above-mentioned (q-zm) block, It may be made to control to perform in parallel processing which writes the data for y blocks in one recording medium to w+1 recording medium, and to perform after that processing which writes data blocked (1-y) in one recording medium in parallel to w recording media. Since the block which free space produces will be at most one piece if it does in this way, the frequency which a contamination saving process generates falls further.
[0017]Or it may be made to control to write in in the turn which each recording medium has where the data for the above-mentioned (q-zm) block is assigned to w+1 recording medium to be shown in drawing 8 (c). This control method is especially effective when "the data which does not need to be rewritten" exists in the block with which the record section used as the write request point belongs. That is, in such a case, the above-mentioned rewriting considers that total with the data which is not required, and the data concerned by which the write request was carried out is data for the above-mentioned (q-zm) block, and controls the address administration control section 42.
[0018]
[Mode for carrying out the invention]Drawing 1 is a block diagram of the recording equipment which applied this invention, and explains the composition below. In the following explanation, data length of a sector is premised on being 16 K bytes for the data length of 512 bytes and a block.
[0019]First, it performs the following data input/output control while giving a start command of the processing concerned to the address administration control section 42, if I/O control unit 41 is received [the processing demand of the writing, read-out, elimination, etc. of data] from the exterior.
[0020]That is, I/O control unit 41 which received the write request of data writes the data inputted from the outside one by one per 512 bytes in two or more buffers 31, 32, 33, and 34. On the other hand, I/O control unit 41 which received the demand of read-out of data reads subsequent data from two or more buffers 31, 32, 33, and 34 per 512 bytes, and outputs it outside.
[0021]According to the processing start command from above-mentioned I/O control unit 41, the address administration control section 42 Control of the data transfer between two or more flash memories 21, 22, 23, and 24 and two or more buffers 31, 32, 33, and 34, Control of the data erasure to two or more flash memories 21, 22, 23, and 24 and management of the data currently

written in two or more flash memories 21, 22, 23, and 24 are performed (it mentions later for details).
[0022]The selector 43 changes connection of the data bus between two or more flash memories 21, 22, 23, and 24 and two or more buffers 31, 32, 33, and 34 according to the connection switching signal from the above-mentioned address administration control section 42.
[0023]Here, the data writing control method which the above-mentioned address administration control section 42 performs is divided roughly into the following two patterns. Namely, one is the control method (henceforth "the 1st data writing control method") at the time of receiving a data writing demand to the logical address field where data is not yet written in, Another is the control method (henceforth "the 2nd data writing control method") at the time of receiving a data writing demand to the logical address field where data is already written in.
[0024]Hereafter, these data writing control method is explained in detail.
[The data writing control method which is the 1] First, when a data writing demand is received to the logical address field where data is not written in, data writing is performed in parallel to the four flash memories 21, 22, 23, and 24 like the above-mentioned former. however, in this invention, the size of the data which is the write-in object concerned shows to drawing 2 (a) - (c) -- as -- the flash memories 21, 22, 23, and 24 -- the writing control methods to each final block differ.
[0025]For example, when the size of the data which is a write-in object is 64 K bytes, although this data is written in the four flash memories 21, 22, 23, and 24 in parallel, free space is produced in neither of those final blocks B21, B22, B23, and B24. This is because the above-mentioned 64 K bytes of data is equivalent to 4 blocks and it is in agreement with total of the final blocks B21, B22, B23, and B24.
[0026]Therefore, the address administration control section 42 in this case is controlled to write in the data 0-127 in parallel to the four final blocks B21, B22, B23, and B24 to be shown in drawing 2 (a) (this write-in form is hereafter called "4-block writing").
[0027]moreover -- if this data is written in the four flash memories 21, 22, 23, and 24 in parallel when the size of the data which is a write-in object is 32 K bytes -- those final blocks B21, B22, B23, and B24 -- it is alike, respectively and 1/2-block free space occurs. This is because the above-mentioned 32 K bytes of data is equivalent to 2 blocks and it is [of total of the final blocks B21, B22, B23, and B24] in agreement with 1/2.
[0028]Therefore, the address administration control section 42 in this case is controlled to write in the data 0-63 in parallel only to the two final blocks B21 and B22 to be shown in drawing 2 (b). That is, about the writing to the final blocks B21, B22, B23, and B24, the degree of parallel is restricted to 2 from 4 on the relation which prevents free space from producing (this write-in form is hereafter called "2-block writing").
[0029]Here, when the size of the data which is a write-in object is 24 K bytes, free space cannot be prevented from producing in a final block even if it restricts the degree of parallel like [in the above-mentioned 32 K bytes]. This is because the above-mentioned 24 K bytes of data is equivalent to 1.5 blocks and it is not in agreement with the integral multiple of a block.
[0030]Therefore, to be shown in drawing 2 (c), the address administration control section 42 in this case controls the data 0-47 to become parallel writing as much as possible so that the final block which free space produces will be only one piece.
[0031]Namely, after writing in the data 0-31 for 1 block in parallel to the two final blocks B21 and B22, The fractional datas 32-47 for remaining 0.5 block are individually written in to the one final block B21 (this write-in form is hereafter called "1.5-block writing"). "It writes in

individually" means performing parallel writing with the degree 1 of parallel.
[0032]As mentioned above, the address administration control section 42 distinguishes the control method according to the size of the data which is a write-in object, and explains the distinction technique hereafter.
[0033]first -- **(ing) size of all the data by which the write request was carried out in the size p of the above-mentioned block of the size q of these data of all the, when size of m and a block is set to p for the number of q and flash memories -- zm+w+y (the integer of z:0 <=z, the integer of w:0 <=w<m, y:0<=y<1) -- a quotient is obtained.
[0034]Here, the degree of parallel means the block count of m, and, as for the above zm, above-mentioned w+y means the block count to which the degree of parallel does not result in m. That is, when it explains using drawing 6, the number of the blocks shown by hatching on the left of an alternate long and short dash line is equivalent to the above zm, and the number of the blocks shown by hatching on the right of an alternate long and short dash line is equivalent to above-mentioned w+y (in addition, w corresponds to the block B1 and y corresponds to block B-2).
[0035]Therefore, the address administration control section 42 is controlled to write in the data for zm block in parallel to m flash memories, and to write in the data for a q-zm block after that to the flash memory of w+1 (at however, the time of y= 0 w) individual. However, it faces writing in the data for this (q-zm) block, Processing which writes the data for y blocks in one flash memory is performed in parallel to w+1 flash memory, and processing which writes data blocked (1-y) in one flash memory is performed in parallel to w flash memories after that.
[0036]A control procedure in case 1 block writes in 152 K bytes of data to four flash memories under the situation of being 16 K bytes, as an example of the above-mentioned distinction technique hereafter (in the case of p= 16, m= 4, and q= 152) is explained.
[0037]First, as for 2 and w, as for it, since q/p=zm+w+y is 152/16=2x4+1+0.5, z turns out that 1 and y are 0.5.
[0038]Therefore, the data for 2 blocks is written in in parallel to four flash memories, and the data for 1.5 blocks is written in to two flash memories after that. However, it faces writing in the data for these 1.5 blocks, Processing which writes the data for 0.5 block in one flash memory is performed in parallel to two flash memories, and processing which writes data blocked (1-0.5) in one flash memory is performed in parallel to one flash memory after that. That is, when it says by drawing 6, the data for 0.5 block will be written in in parallel to the block B1 and each B-2, and the data for 0.5 block will be individually written in only to the block B1 after that.
[0039]Here, in the size p of all the data by which the write request was carried out, although 152 K bytes and the size q of a block were explained as 16 K bytes, a unit of these sizes p and q is not limited to a byte. For example, the effect same also as 32 sectors as the above is acquired [size / p / of all the data by which the write request was carried out] in 304 sectors and the size q of a block.
[0040]As explained above, according to this invention, a block which free space produces will be at most one piece. If it is total and sees by this as a result of the fall of frequency which a contamination saving process generates, it is possible to raise write-in performance to a flash memory.
[0041]But according to this invention, the degree of parallel may be restricted, and a fall of drawing speed is caused at this point. However, it is only about a final block that the degree of parallel is restricted, and since it is made to perform parallel writing as much as possible also about this final block, even if the degree of parallel is restricted as mentioned above, influence on that drawing speed is very small.

[0042]in addition -- the above-mentioned explanation -- flash memory 21->22->23->24->21-> -- although operation which performs parallel writing in order of ... was explained, this invention is not limited to this. That is, since there is variation in hardware ability of each flash memory, there is variation also in time which each writing processing takes. Therefore, it is preferred to control sequentially from a flash memory which did not perform parallel writing as mentioned above, but writing processing ended early to write in the following data.
[0043]As shown in drawing 2 (b) and (c), when the sizes of the data which is a write-in object are 32 K bytes and 24 K bytes, the period when the degree of parallel is restricted to 2, i.e., the period when parallel writing processing is performed only to the two flash memories 21 and 22, exists. Therefore, when an uneliminated field exists in remaining two flash memories 23-24, it is preferred to perform erasing processing of this field in parallel to the writing processing to the above-mentioned flash memories 21 and 22.
[0044]In the above-mentioned explanation, it faces writing in data blocked (q-zm), Processing which writes the data for y blocks in one flash memory is performed in parallel to w+1 flash memory, Then, although processing which writes data blocked (1-y) in one flash memory is performed in parallel to w flash memories, this invention is not limited to this. That is, it may be made to write in the data for the above-mentioned (q-zm) block in parallel to w+1 flash memory, as shown in drawing 8 (a).
[0045]But if it does in this way, the number of the blocks which free space produces may be two or more pieces. However, it cannot be overemphasized that the number decreases compared with the case where the above-mentioned conventional technology is applied.
[0046]By the way, in order to read or rewrite the data written in in parallel as mentioned above, the address administration control section 42 must generalize and manage the data writing state in the flash memories 21, 22, 23, and 24 concerned. Namely, the address administration control section 42 generates the block managing table (refer to drawing 3) provided with the following fields for every logic address block by which an access request is carried out from the outside.
[0047]First, the field where the degree field of parallel shows to how many flash memories data was written in in parallel is said. That is, as shown in drawing 3 (a), "4" is set to the degree field of parallel of the logic address block written in 4 blocks as mentioned above. On the other hand, as mentioned above, as shown in drawing 3 (b) and (c), "2" is set to 2-block writing and the degree field of parallel of a logic address block written in 1.5 blocks. "0" is set to the degree field of parallel of the logic address block which is a non-writing area.
[0048]Next, the field where the un-parallel sector number field shows the number of sectors with which parallel writing is not performed among 32 sectors contained in the logic address block concerned is said. That is, as mentioned above, as shown in drawing 3 (a) and (b), "0" is set to 4-block writing and the un-parallel sector number field of a logic address block written in 2 blocks. As shown in drawing 3 (c), "16" is set to the un-parallel sector number field of a logic address block written in 1.5 blocks as mentioned above on the other hand.
[0049]Next, the field where the flash memory appointed field shows a flash memory in which the logic address block concerned exists is said. For example, "0" is set to the flash memory appointed field of a logic address block which exists in the above-mentioned flash memory 21, and "1" is set to the flash memory appointed field of a logic address block which exists in the above-mentioned flash memory 22. "2" is set to the flash memory appointed field of a logic address block which exists in the above-mentioned flash memory 23, and "3" is set to the flash memory appointed field of a logic address block which exists in the above-mentioned flash memory 24.

[0050]Next, the field where a physical address field shows the physical address corresponding to the logic address block concerned is said. Of course, the physical address set as this field is a physical address in the flash memory shown in the above-mentioned flash memory appointed field.
[0051]Next, the field where the sector column management information field expressed the turn of parallel writing per sector is said. For example, flash memory 21->22->23->24->21-> ... When parallel writing is performed in order, As shown in drawing 3 (a), as sector column management information corresponding to logical address a "0", "3" will be located [as sector column management information corresponding to the logical address a+1 / as sector column management information corresponding to the logical address a+2 in "1"] in a line, respectively as sector column management information corresponding to the logical address a+3 in "2."
[The data writing control method which is the 2] By the way, it is usual that the data written in a flash memory is a series of image data and music data (1 graphics file and first-sound easy file). Therefore, also when eliminating the data written in the flash memory, a possibility of eliminating collectively a series of image data and music data (namely, data written in continuously) is high. So, in data writing control of the above 1st, it is supposed that parallel writing is performed as much as possible from a viewpoint in which drawing speed is not reduced.
[0052]However, when it is more total to write in individually and sees rather than performing parallel writing as much as possible like a data writing control method of the above 1st, there is also a scene whose write-in performance to a flash memory improves.
[0053]For example, in editing work of music data written in a flash memory, there is a case where he would like to rewrite some data written in continuously. In this case, it is better to write data which is a candidate for rewriting in one block, as shown in drawing 7 (b) as a hatching field rather than written in over two or more blocks, as shown in drawing 7 (a) as a hatching field. Because, it is for what is necessary being to involve in about one block and just to carry out a saving process in a scene shown in drawing 7 (b), to involving in about four blocks and carrying out a saving process in a scene shown in drawing 7 (a).
[0054]Since it is such, after writing successive data in two or more flash memories in parallel by the data writing control method of the above 1st, when a part of this successive data needs to be rewritten, it should be preferred to adopt the following control methods.
[0055]First, the address administration control section 42 which received the data writing demand, By referring to the contents of the above-mentioned block managing table, this data writing demand, It is judged any of the demand (it may be called the following "a data rewrite demand") for rewriting some successive data, or the demand (it may be called the following "new data write request") for writing in successive data newly they are. Namely, if it is the data writing demand to the logical address field to which data is already written in, It judges that the data writing demand concerned is a data rewrite demand, and on the other hand, if it is the data writing demand to the logical address field to which data is not yet written in, it will be judged that the data writing demand concerned is a new data write request.
[0056]And the data writing control method of the above 1st is used for the address administration control section 42 judged that the data writing demand concerned is a new data write request. On the other hand, the address administration control section 42 judged that the data writing demand concerned is a data rewrite demand judges whether the data for which rewriting is not required in the block with which the data which is a candidate for rewriting belongs further exists.

[0057]For example, under the situation where 1.5 blocks of data 0-47 is written in the flash memories 21 and 22 as shown in drawing 4, When there is a demand for rewriting the data 32-47, the data 0-31 (however, except for odd number) for which rewriting is not required in the block with which the data 32-47 belongs exists. Therefore, the address administration control section 42 in this case will judge "the data which does not need to be rewritten exists", and performs the following control.
[0058]First, the address administration control section 42 considers that the data for 1.5 blocks which are total with the data 0-31 (32 sector data) which does not need to be rewritten, and the data 32-47 (16 sector data) concerned by which the write request was carried out is data for the above-mentioned (q-zm) block. At this time, it cannot be overemphasized that w is 1 and y is 0.5.
[0059]And the address administration control section 42 is in the state which assigned the data for this (q-zm) block to the w+1 flash memories 23 and 24, and is controlled to write in in the turn (here turn of 23->24) which each flash memories 23 and 24 have. Namely, once reading the data 0-31 currently written in in parallel to two blocks to the buffer 33, It rewrites individually to the eliminated field of the flash memory 23, and controls to write the data 32-47 in the eliminated field of the flash memory 24 individually subsequently. This data 32-47 is passed from the exterior to the address administration control section 42 via I/O control unit 41 and the buffer 34.
[0060]As mentioned above, according to the 2nd data writing control, successive data will be located as much as possible in a line with the block on the flash memory 23-24. Thus, when setting and the data 0-31 or the data 32-47 needs to be rewritten again, a contamination saving process is not generated.
[0061]Above, only operation when the address administration control section 42 judges "the data which does not need to be rewritten exists" was explained. That is, although reference is not made about operation when the address administration control section 42 judges "the data which does not need to be rewritten does not exist", the data writing control method of the above 1st is used for the address administration control section 42 at the time of judging in this way.
[0062]This is because "the data which does not need to be rewritten does not exist" means rewriting all of data. For example, that there is a data writing demand for 2 blocks to a 1.5-block field means that the data for [former] 1.5 blocks is unnecessary. Therefore, it is appropriate to such a data writing demand to think that it is the demand for writing in successive data newly.
[0063]It is shown in drawing 5 how at the end, the contents of the block managing table change by the 2nd above-mentioned example of data writing control. About field composition or setup information, since it is the same as data writing control of the above 1st, explanation is omitted here.

2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

TECHNICAL FIELD

[A field of the invention to which invention belongs] This invention relates to recording equipment for recording data on recording media, such as a flash memory, especially about recording equipment for recording data.

PRIOR ART

[Description of the Prior Art]It is common that backup by ** cell with high ** portability which can rewrite ** data, etc. uses recording media, such as a flash memory, from unnecessary Reasons in the recording equipment of the portable device which deals with music data and picture image data.
[0003]However, according to the present flash memory, there was a problem that waiting time arose, on the occasion of data writing. The direction of time required for the Reason to write the data transmitted to the buffer in this way than time required to transmit the data which is a write-in object to the buffer in recording equipment in a flash memory from the buffer concerned is because it is substantially long.
[0004]Then, JP,2000-132982,A has disclosed recording equipment provided with two or more flash memories. According to such recording equipment, since data writing can be performed in parallel to two or more flash memories, the above-mentioned problem that waiting time arises is not generated.

[Translation done.] * NOTICES *

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precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

TECHNICAL PROBLEM

[Problem to be solved by the invention]By the way, generally, the data writing unit to a flash memory is called a sector, and the data erasure (it mentions later) unit on a flash memory is called a block. That is, as shown in drawing 9 (a), the data in a flash memory is managed in the unit of the block which consists of 32 sectors (the data length of a sector explains the data length of 512 bytes and a block as 16 K bytes hereafter).
[0006]Only the data rewrite of one way can be performed, i.e., there is the feature that the value of data cannot be rewritten from 1 to 0 (or 0-1) in a flash memory. Therefore, in order to perform data writing, it is necessary to change all the values of the data in the field used as that writing destination into 1 (or 0) (this conversion process is hereafter called "erasing processing".). The field which this erasing processing has completed is called "eliminated field", and the field which has not been completed is called "uneliminated field."
[0007]When rewriting the data 0-15 within the block A shown in drawing 9 (b) from the above situation, as shown in drawing 9 (c), the data 16-31 which does not need to be rewritten is once first read from flash memory F1 to the buffer B. And as shown the data 16-31 read to the buffer B in this way in drawing 9 (d), after rewriting to the eliminated field E of another flash memory F2, erasing processing is performed about the field of the above-mentioned block A.
[0008]A series of above-mentioned processings (namely, processing for the data 16-31 which does not need to be rewritten not to be involved in the rewriting processing concerned) are called a contamination saving process, and have become a major factor which reduces the drawing speed to a flash memory. Although the after-rewriting data 0-15 shown in drawing 9 (d) is passed to the recording equipment concerned from the exterior, it omits detailed explanation about this point here.
[0009]Here, since data writing can be performed in parallel to two or more flash memories according to the recording equipment indicated by JP,2000-132982,A as described above, the above-mentioned problem that waiting time arises is not generated. However, when data writing was performed in parallel to two or more flash memories in this way, SUBJECT that the frequency which is involved in in the case of data erasure and a saving process generates became high occurred.
[0010]Namely, when writing a certain music data M1 in a flash memory and the data size is not an integral multiple of x (size which is 1 block of a flash memory) (number of a flash memory), as shown in drawing 10, Free space occurs in each final block (it mentions later) B1 - B4 of flash memory F1 - F4. Then, when writing another music data M2 in the flash memory F1 concerned - F4, as a result of writing in this music data M2 from the free space of the above-mentioned final block B1 - B4, the separate music data M1 and M2 will exist in the same block. Therefore, when all of the music data M1 need to be eliminated in this state, the music data M2 written in the final block B1 - B4 must be evacuated.
[0011]The above-mentioned final block means the block with which the data which is a write-in object will be written in at the end. That is, as shown in drawing 6, if data writing is performed in parallel to m flash memories, free space will not occur in the block shown by hatching on the left of an alternate long and short dash line, but free space may occur in the block shown by hatching

on the right of an alternate long and short dash line. Thus, since the data which is a write-in object is the block which will be written in at the end, the block which free space may generate is carried out to calling especially these blocks a "final block."
[0012]This invention was proposed based on the above-mentioned conventional situation, and is ****. The purpose is to reduce the frequency which is involved in in the recording equipment which performs data writing in parallel to a flash memory, and a saving process generates.

[Translation done.] * NOTICES *

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3.In the drawings, any words are not translated.

MEANS

[Means for solving problem]The following means are used for this invention to achieve the above objects. Namely, as this invention is shown in drawing 1, data writing is performed to the record section which erasing processing has completed, And it is premised on the recording equipment 1 which writes in in parallel the data by which the write request was carried out from the outside to two or more recording media 21, 22, 23, and 24 which bundle up by the predetermined block unit which consists of two or more record sections, and perform data erasure.
[0014]When size of m and the above-mentioned block is set to p for the number of q and the above-mentioned recording media, here the size of all the data by which the write request was carried out from the above-mentioned outside the address administration control section 42, first -- **(ing) size q of all the data by which the write request was carried out from the above-mentioned outside in the size p of the above-mentioned block -- zm+w+y (the integer of z:0 <=z, the integer of w:0 <=w<m, y:0<=y<1) -- a quotient is obtained. And it controls to write in the data for zm block in parallel to m recording media, and to write in data blocked (q-zm) after that to the recording medium of w+1 (at however, the time of y= 0 w) individual.
[0015]For example, the address administration control section 42 is controlled to write in the data for the above-mentioned (q-zm) block in parallel to w+1 recording medium to be shown in drawing 8 (a). If it does in this way, the number of the blocks which free space produces will decrease compared with the case where the above-mentioned conventional technology is applied. It cannot be overemphasized that the frequency which a contamination saving process generates will fall by this.
[0016]Of course, as shown in drawing 8 (b), it faces writing in the data for the above-mentioned (q-zm) block, It may be made to control to perform in parallel processing which writes the data for y blocks in one recording medium to w+1 recording medium, and to perform after that

processing which writes data blocked (1-y) in one recording medium in parallel to w recording media. Since the block which free space produces will be at most one piece if it does in this way, the frequency which a contamination saving process generates falls further.
[0017]Or it may be made to control to write in in the turn which each recording medium has where the data for the above-mentioned (q-zm) block is assigned to w+1 recording medium to be shown in drawing 8 (c). This control method is especially effective when "the data which does not need to be rewritten" exists in the block with which the record section used as the write request point belongs. That is, in such a case, the above-mentioned rewriting considers that total with the data which is not required, and the data concerned by which the write request was carried out is data for the above-mentioned (q-zm) block, and controls the address administration control section 42.
[0018]
[Mode for carrying out the invention]Drawing 1 is a block diagram of the recording equipment which applied this invention, and explains the composition below. In the following explanation, data length of a sector is premised on being 16 K bytes for the data length of 512 bytes and a block.
[0019]First, it performs the following data input/output control while giving a start command of the processing concerned to the address administration control section 42, if I/O control unit 41 is received [the processing demand of the writing, read-out, elimination, etc. of data] from the exterior.
[0020]That is, I/O control unit 41 which received the write request of data writes the data inputted from the outside one by one per 512 bytes in two or more buffers 31, 32, 33, and 34. On the other hand, I/O control unit 41 which received the demand of read-out of data reads subsequent data from two or more buffers 31, 32, 33, and 34 per 512 bytes, and outputs it outside.
[0021]According to the processing start command from above-mentioned I/O control unit 41, the address administration control section 42 Control of the data transfer between two or more flash memories 21, 22, 23, and 24 and two or more buffers 31, 32, 33, and 34, Control of the data erasure to two or more flash memories 21, 22, 23, and 24 and management of the data currently written in two or more flash memories 21, 22, 23, and 24 are performed (it mentions later for details).
[0022]The selector 43 changes connection of the data bus between two or more flash memories 21, 22, 23, and 24 and two or more buffers 31, 32, 33, and 34 according to the connection switching signal from the above-mentioned address administration control section 42.
[0023]Here, the data writing control method which the above-mentioned address administration control section 42 performs is divided roughly into the following two patterns. Namely, one is the control method (henceforth "the 1st data writing control method") at the time of receiving a data writing demand to the logical address field where data is not yet written in, Another is the control method (henceforth "the 2nd data writing control method") at the time of receiving a data writing demand to the logical address field where data is already written in.
[0024]Hereafter, these data writing control method is explained in detail.
[The data writing control method which is the 1] First, when a data writing demand is received to the logical address field where data is not written in, data writing is performed in parallel to the four flash memories 21, 22, 23, and 24 like the above-mentioned former. however, in this invention, the size of the data which is the write-in object concerned shows to drawing 2 (a) - (c) -- as -- the flash memories 21, 22, 23, and 24 -- the writing control methods to each final block

differ.
[0025]For example, when the size of the data which is a write-in object is 64 K bytes, although this data is written in the four flash memories 21, 22, 23, and 24 in parallel, free space is produced in neither of those final blocks B21, B22, B23, and B24. This is because the above-mentioned 64 K bytes of data is equivalent to 4 blocks and it is in agreement with total of the final blocks B21, B22, B23, and B24.
[0026]Therefore, the address administration control section 42 in this case is controlled to write in the data 0-127 in parallel to the four final blocks B21, B22, B23, and B24 to be shown in drawing 2 (a) (this write-in form is hereafter called "4-block writing").
[0027]moreover -- if this data is written in the four flash memories 21, 22, 23, and 24 in parallel when the size of the data which is a write-in object is 32 K bytes -- those final blocks B21, B22, B23, and B24 -- it is alike, respectively and 1/2-block free space occurs. This is because the above-mentioned 32 K bytes of data is equivalent to 2 blocks and it is [of total of the final blocks B21, B22, B23, and B24] in agreement with 1/2.
[0028]Therefore, the address administration control section 42 in this case is controlled to write in the data 0-63 in parallel only to the two final blocks B21 and B22 to be shown in drawing 2 (b). That is, about the writing to the final blocks B21, B22, B23, and B24, the degree of parallel is restricted to 2 from 4 on the relation which prevents free space from producing (this write-in form is hereafter called "2-block writing").
[0029]Here, when the size of the data which is a write-in object is 24 K bytes, free space cannot be prevented from producing in a final block even if it restricts the degree of parallel like [in the above-mentioned 32 K bytes]. This is because the above-mentioned 24 K bytes of data is equivalent to 1.5 blocks and it is not in agreement with the integral multiple of a block.
[0030]Therefore, to be shown in drawing 2 (c), the address administration control section 42 in this case controls the data 0-47 to become parallel writing as much as possible so that the final block which free space produces will be only one piece.
[0031]Namely, after writing in the data 0-31 for 1 block in parallel to the two final blocks B21 and B22, The fractional datas 32-47 for remaining 0.5 block are individually written in to the one final block B21 (this write-in form is hereafter called "1.5-block writing"). "It writes in individually" means performing parallel writing with the degree 1 of parallel.
[0032]As mentioned above, the address administration control section 42 distinguishes the control method according to the size of the data which is a write-in object, and explains the distinction technique hereafter.
[0033]first -- **(ing) size of all the data by which the write request was carried out in the size p of the above-mentioned block of the size q of these data of all the, when size of m and a block is set to p for the number of q and flash memories -- zm+w+y (the integer of z:0 <=z, the integer of w:0 <=w<m, y:0<=y<1) -- a quotient is obtained.
[0034]Here, the degree of parallel means the block count of m, and, as for the above zm, above-mentioned w+y means the block count to which the degree of parallel does not result in m. That is, when it explains using drawing 6, the number of the blocks shown by hatching on the left of an alternate long and short dash line is equivalent to the above zm, and the number of the blocks shown by hatching on the right of an alternate long and short dash line is equivalent to above-mentioned w+y (in addition, w corresponds to the block B1 and y corresponds to block B-2).
[0035]Therefore, the address administration control section 42 is controlled to write in the data for zm block in parallel to m flash memories, and to write in the data for a q-zm block after that to the flash memory of w+1 (at however, the time of y= 0 w) individual. However, it faces

writing in the data for this (q-zm) block, Processing which writes the data for y blocks in one flash memory is performed in parallel to w+1 flash memory, and processing which writes data blocked (1-y) in one flash memory is performed in parallel to w flash memories after that.
[0036]A control procedure in case 1 block writes in 152 K bytes of data to four flash memories under the situation of being 16 K bytes, as an example of the above-mentioned distinction technique hereafter (in the case of p= 16, m= 4, and q= 152) is explained.
[0037]First, as for 2 and w, as for it, since q/p=zm+w+y is 152/16=2x4+1+0.5, z turns out that 1 and y are 0.5.
[0038]Therefore, the data for 2 blocks is written in in parallel to four flash memories, and the data for 1.5 blocks is written in to two flash memories after that. However, it faces writing in the data for these 1.5 blocks, Processing which writes the data for 0.5 block in one flash memory is performed in parallel to two flash memories, and processing which writes data blocked (1-0.5) in one flash memory is performed in parallel to one flash memory after that. That is, when it says by drawing 6, the data for 0.5 block will be written in in parallel to the block B1 and each B-2, and the data for 0.5 block will be individually written in only to the block B1 after that.
[0039]Here, in the size p of all the data by which the write request was carried out, although 152 K bytes and the size q of the block were explained as 16 K bytes, the unit of these sizes p and q is not limited to a byte. For example, the effect same also as 32 sectors as the above is acquired [size / p / of all the data by which the write request was carried out] in 304 sectors and the size q of a block.
[0040]As explained above, according to this invention, the block which free space produces will be at most one piece. If it is total and sees by this as a result of the fall of frequency which a contamination saving process generates, it is possible to raise the write-in performance to a flash memory.
[0041]But according to this invention, the degree of parallel may be restricted, and the fall of drawing speed is caused at this point. However, it is only about a final block that the degree of parallel is restricted, and since it is made to perform parallel writing as much as possible also about this final block, even if the degree of parallel is restricted as mentioned above, the influence on that drawing speed is very small.
[0042]in addition -- the above-mentioned explanation -- flash memory 21->22->23->24->21-> -- although the operation which performs parallel writing in order of ... was explained, this invention is not limited to this. That is, since there is variation in the hardware ability of each flash memory, there is variation also in the time which each writing processing takes. Therefore, it is preferred to control sequentially from the flash memory which did not perform parallel writing as mentioned above, but writing processing ended early to write in the following data.
[0043]As shown in drawing 2 (b) and (c), when the sizes of the data which is a write-in object are 32 K bytes and 24 K bytes, the period when the degree of parallel is restricted to 2, i.e., the period when parallel writing processing is performed only to the two flash memories 21 and 22, exists. Therefore, when an uneliminated field exists in remaining two flash memories 23-24, it is preferred to perform erasing processing of this field in parallel to the writing processing to the above-mentioned flash memories 21 and 22.
[0044]In the above-mentioned explanation, it faces writing in data blocked (q-zm), Processing which writes the data for y blocks in one flash memory is performed in parallel to w+1 flash memory, Then, although processing which writes data blocked (1-y) in one flash memory is performed in parallel to w flash memories, this invention is not limited to this. That is, it may be made to write in the data for the above-mentioned (q-zm) block in parallel to w+1 flash memory,

as shown in drawing 8 (a).
[0045]But if it does in this way, the number of the blocks which free space produces may be two or more pieces. However, it cannot be overemphasized that the number decreases compared with the case where the above-mentioned conventional technology is applied.
[0046]By the way, in order to read or rewrite the data written in in parallel as mentioned above, the address administration control section 42 must generalize and manage the data writing state in the flash memories 21, 22, 23, and 24 concerned. Namely, the address administration control section 42 generates the block managing table (refer to drawing 3) provided with the following fields for every logic address block by which an access request is carried out from the outside.
[0047]First, the field where the degree field of parallel shows to how many flash memories data was written in in parallel is said. That is, as shown in drawing 3 (a), "4" is set to the degree field of parallel of the logic address block written in 4 blocks as mentioned above. On the other hand, as mentioned above, as shown in drawing 3 (b) and (c), "2" is set to 2-block writing and the degree field of parallel of a logic address block written in 1.5 blocks. "0" is set to the degree field of parallel of the logic address block which is a non-writing area.
[0048]Next, the field where the un-parallel sector number field shows the number of sectors with which parallel writing is not performed among 32 sectors contained in the logic address block concerned is said. That is, as mentioned above, as shown in drawing 3 (a) and (b), "0" is set to 4-block writing and the un-parallel sector number field of a logic address block written in 2 blocks. As shown in drawing 3 (c), "16" is set to the un-parallel sector number field of the logic address block written in 1.5 blocks as mentioned above on the other hand.
[0049]Next, the field where the flash memory appointed field shows the flash memory in which the logic address block concerned exists is said. For example, "0" is set to the flash memory appointed field of the logic address block which exists in the above-mentioned flash memory 21, and "1" is set to the flash memory appointed field of the logic address block which exists in the above-mentioned flash memory 22. "2" is set to the flash memory appointed field of the logic address block which exists in the above-mentioned flash memory 23, and "3" is set to the flash memory appointed field of the logic address block which exists in the above-mentioned flash memory 24.
[0050]Next, the field where a physical address field shows the physical address corresponding to the logic address block concerned is said. Of course, the physical address set as this field is a physical address in the flash memory shown in the above-mentioned flash memory appointed field.
[0051]Next, the field where the sector column management information field expressed the turn of parallel writing per sector is said. For example, flash memory 21->22->23->24->21-> ... When parallel writing is performed in order, As shown in drawing 3 (a), as sector column management information corresponding to logical address a "0", "3" will be located [as sector column management information corresponding to the logical address a+1 / as sector column management information corresponding to the logical address a+2 in "1"] in a line, respectively as sector column management information corresponding to the logical address a+3 in "2."
[The data writing control method which is the 2] By the way, it is usual that the data written in a flash memory is a series of image data and music data (1 graphics file and first-sound easy file). Therefore, also when eliminating the data written in the flash memory, a possibility of eliminating collectively a series of image data and music data (namely, data written in continuously) is high. So, in data writing control of the above 1st, it is supposed that parallel writing is performed as much as possible from a viewpoint in which drawing speed is not

reduced.
[0052]However, when it is more total to write in individually and sees rather than performing parallel writing as much as possible like the data writing control method of the above 1st, there is also a scene whose write-in performance to a flash memory improves.
[0053]For example, in the editing work of the music data written in the flash memory, there is a case where he would like to rewrite some data written in continuously. In this case, it is better to write the data which is a candidate for rewriting in one block, as shown in drawing 7 (b) as a hatching field rather than written in over two or more blocks, as shown in drawing 7 (a) as a hatching field. Because, it is for what is necessary being to involve in about one block and just to carry out a saving process in the scene shown in drawing 7 (b), to involving in about four blocks and carrying out a saving process in the scene shown in drawing 7 (a).
[0054]Since it is such, after writing successive data in two or more flash memories in parallel by the data writing control method of the above 1st, when a part of this successive data needs to be rewritten, it should be preferred to adopt the following control methods.
[0055]First, the address administration control section 42 which received the data writing demand, By referring to the contents of the above-mentioned block managing table, this data writing demand, It is judged any of the demand (it may be called the following "a data rewrite demand") for rewriting some successive data, or the demand (it may be called the following "new data write request") for writing in successive data newly they are. Namely, if it is the data writing demand to the logical address field to which data is already written in, It judges that the data writing demand concerned is a data rewrite demand, and on the other hand, if it is the data writing demand to the logical address field to which data is not yet written in, it will be judged that the data writing demand concerned is a new data write request.
[0056]And the data writing control method of the above 1st is used for the address administration control section 42 judged that the data writing demand concerned is a new data write request. On the other hand, the address administration control section 42 judged that the data writing demand concerned is a data rewrite demand judges whether the data for which rewriting is not required in the block with which the data which is a candidate for rewriting belongs further exists.
[0057]For example, under the situation where 1.5 blocks of data 0-47 is written in the flash memories 21 and 22 as shown in drawing 4, When there is a demand for rewriting the data 32-47, the data 0-31 (however, except for odd number) for which rewriting is not required in the block with which the data 32-47 belongs exists. Therefore, the address administration control section 42 in this case will judge "the data which does not need to be rewritten exists", and performs the following control.
[0058]First, the address administration control section 42 considers that the data for 1.5 blocks which are total with the data 0-31 (32 sector data) which does not need to be rewritten, and the data 32-47 (16 sector data) concerned by which the write request was carried out is data for the above-mentioned (q-zm) block. At this time, it cannot be overemphasized that w is 1 and y is 0.5.
[0059]And the address administration control section 42 is in the state which assigned the data for this (q-zm) block to the w+1 flash memories 23 and 24, and is controlled to write in in the turn (here turn of 23->24) which each flash memories 23 and 24 have. Namely, once reading the data 0-31 currently written in in parallel to two blocks to the buffer 33, It rewrites individually to the eliminated field of the flash memory 23, and controls to write the data 32-47 in the eliminated field of the flash memory 24 individually subsequently. This data 32-47 is passed

from the exterior to the address administration control section 42 via I/O control unit 41 and the buffer 34.
[0060]As mentioned above, according to the 2nd data writing control, successive data will be located as much as possible in a line with a block on the flash memory 23-24. Thus, when setting and the data 0-31 or the data 32-47 needs to be rewritten again, a contamination saving process is not generated.
[0061]Above, only operation when the address administration control section 42 judges "data which does not need to be rewritten exists" was explained. That is, although reference is not made about operation when the address administration control section 42 judges "data which does not need to be rewritten does not exist", a data writing control method of the above 1st is used for the address administration control section 42 at the time of judging in this way.
[0062]This is because "data which does not need to be rewritten does not exist" means rewriting all of data. For example, that there is a data writing demand for 2 blocks to a 1.5-block field means that data for [former] 1.5 blocks is unnecessary. Therefore, it is appropriate to such a data writing demand to think that it is the demand for writing in successive data newly.
[0063]It is shown in drawing 5 how at the end, the contents of the block managing table change by the 2nd above-mentioned example of data writing control. About field composition or setup information, since it is the same as data writing control of the above 1st, explanation is omitted here.

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1]The block diagram of the recording equipment which applied this invention
[Drawing 2]The explanatory view of the 1st data writing control method
[Drawing 3]The constitutional diagram of the block managing table at the time of the 1st data writing control
[Drawing 4]The explanatory view of the 2nd data writing control method
[Drawing 5]The constitutional diagram of the block managing table at the time of the 2nd data writing control
[Drawing 6]The explanatory view of the distinction technique of the data writing control method
[Drawing 7]The explanatory view of a data rewrite
[Drawing 8](q-zm) The figure showing the write-in mode of blocked data
[Drawing 9]The explanatory view of a block sector and a contamination saving process

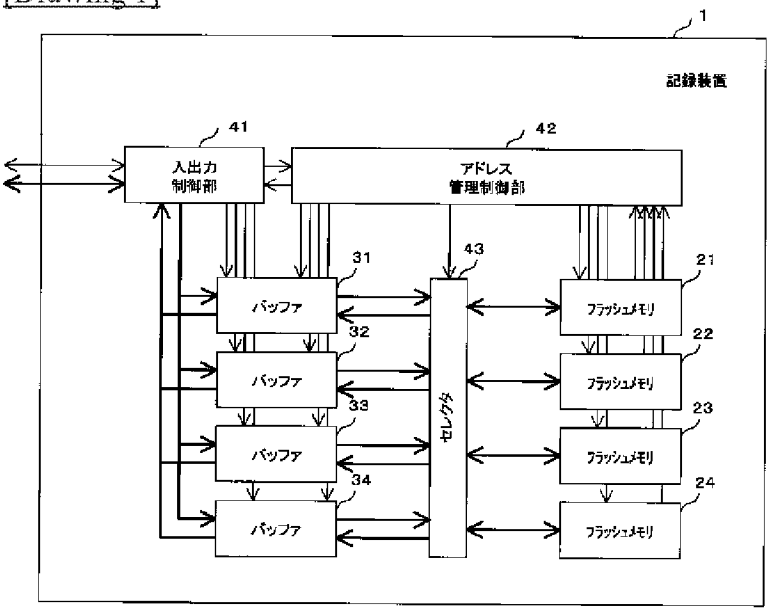
[Drawing 10]The explanatory view of the block with which separate data exists
[Explanations of letters or numerals]
1 Recording equipment
21 Flash memory
22 Flash memory
23 Flash memory
24 Flash memory
31 Buffer
32 Buffer
33 Buffer
34 Buffer
41 I/O control unit
42 Address administration control section
43 Selector

[Translation done.] * NOTICES *

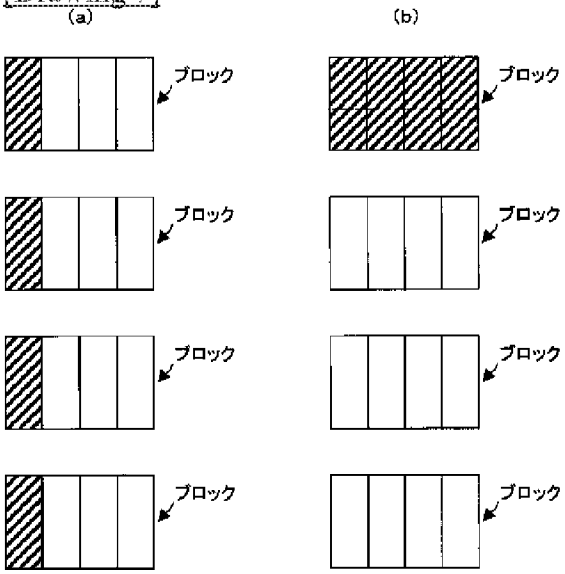
1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DRAWINGS

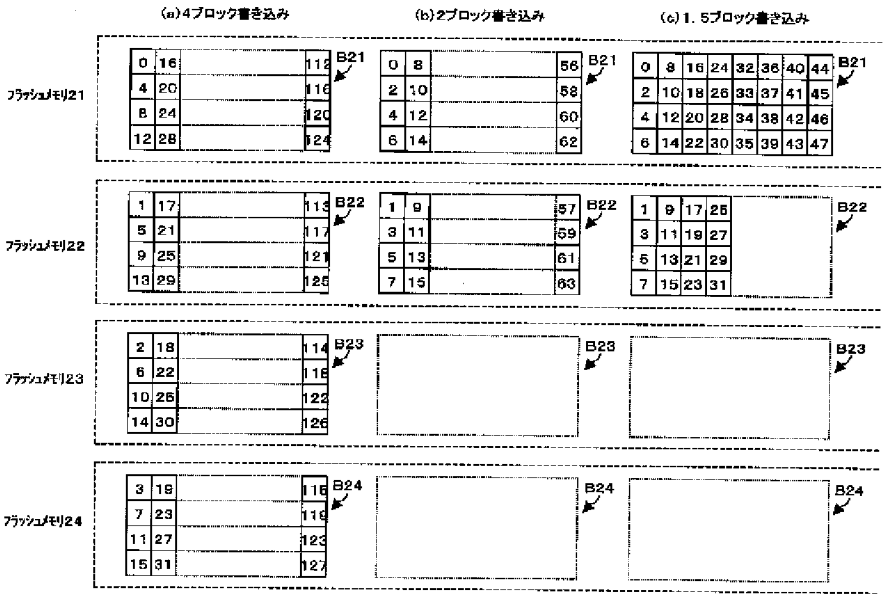
[Drawing 1]



[Drawing 7]



[Drawing 2]



[Drawing 3]

(a)4ブロック書き込み

論理アドレス	並列度	非並列セクタ数	フラッシュメモリ指定	物理アドレス	セクタ列管理情報
a	4	0	0	A	0,0,0,.....,0
a+1	4	0	1	B	1,1,1,.....,1
a+2	4	0	2	C	2,2,2,.....,2
a+3	4	0	3	D	3,3,3,.....,3

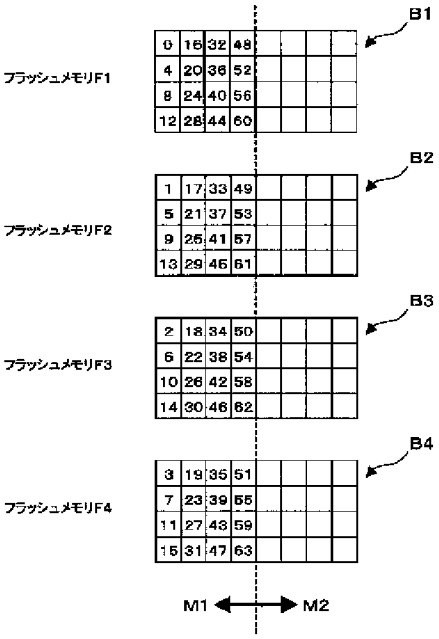
(b)2ブロック書き込み

論理アドレス	並列度	非並列セクタ数	フラッシュメモリ指定	物理アドレス	セクタ列管理情報
b	2	0	0	E	0,0,0,.....,0
b+1	2	0	1	F	1,1,1,.....,1

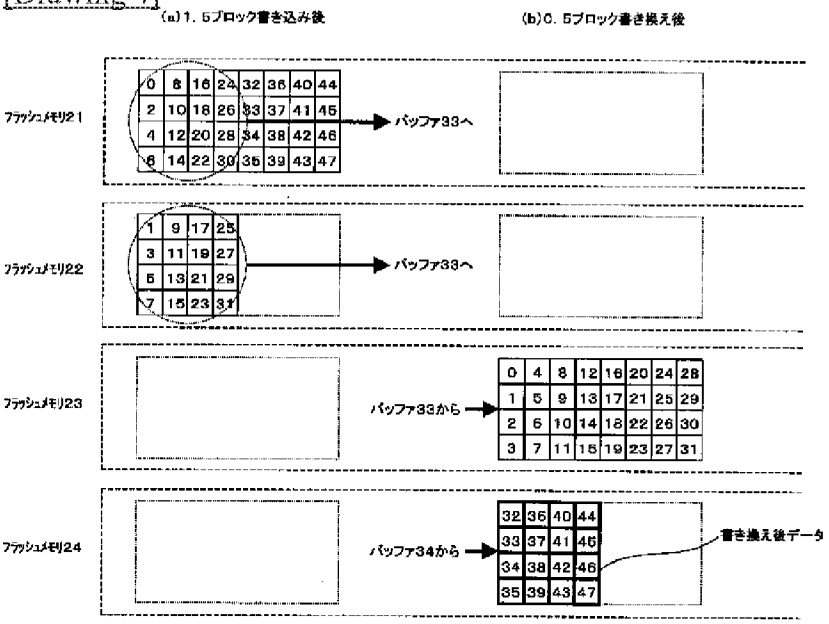
(c)1.5ブロック書き込み

論理アドレス	並列度	非並列セクタ数	フラッシュメモリ指定	物理アドレス	セクタ列管理情報
c	2	16	0	G	0,0,0,.....,0
c+1	2	16	1	H	1,1,1,.....,1

[Drawing 10]



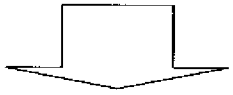
[Drawing 4]



[Drawing 5]

(a)1.5ブロック書き込み後

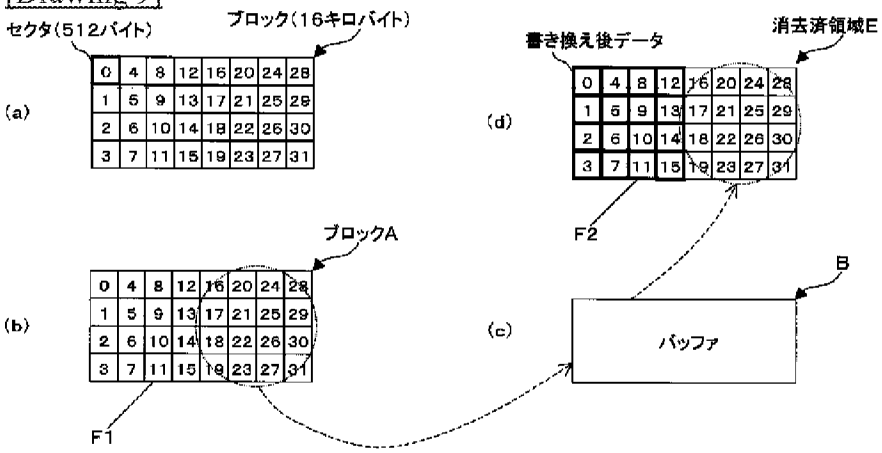
論理アドレス	並列度	非並列セクタ数	フラッシュメモリ指定	物理アドレス	セクタ列管理情報
c	2	16	0	G	0,0,0,.....,0
c+1	2	16	1	H	1,1,1,.....,1



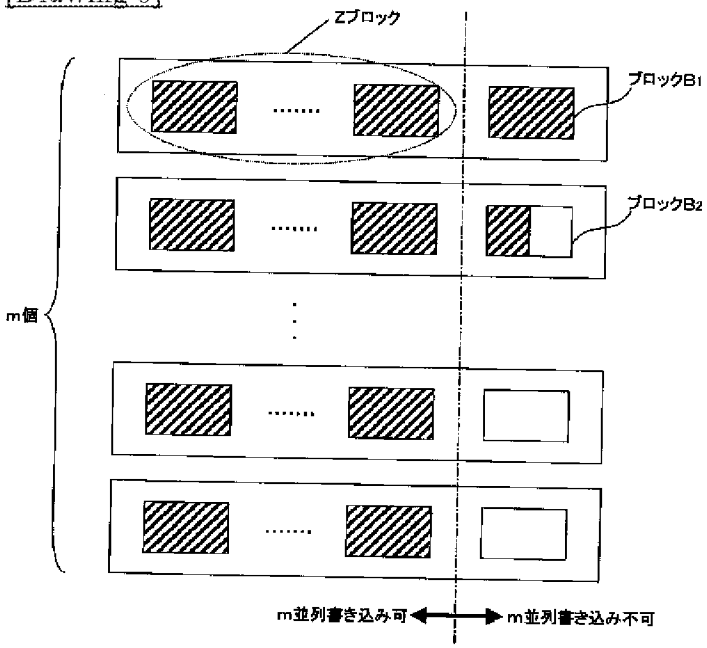
(b)0.5ブロック書き換え後

論理アドレス	並列度	非並列セクタ数	フラッシュメモリ指定	物理アドレス	セクタ列管理情報
c	1	0	2	I	0,0,0,.....,0
c+1	1	0	3	J	0,0,0,.....,0

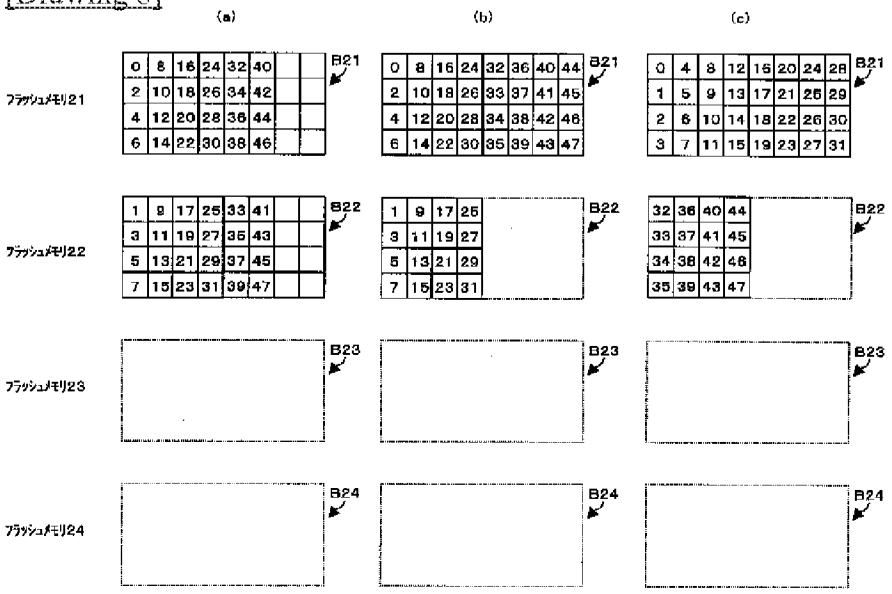
[Drawing 9]



[Drawing 6]



[Drawing 8]



[Translation done.]